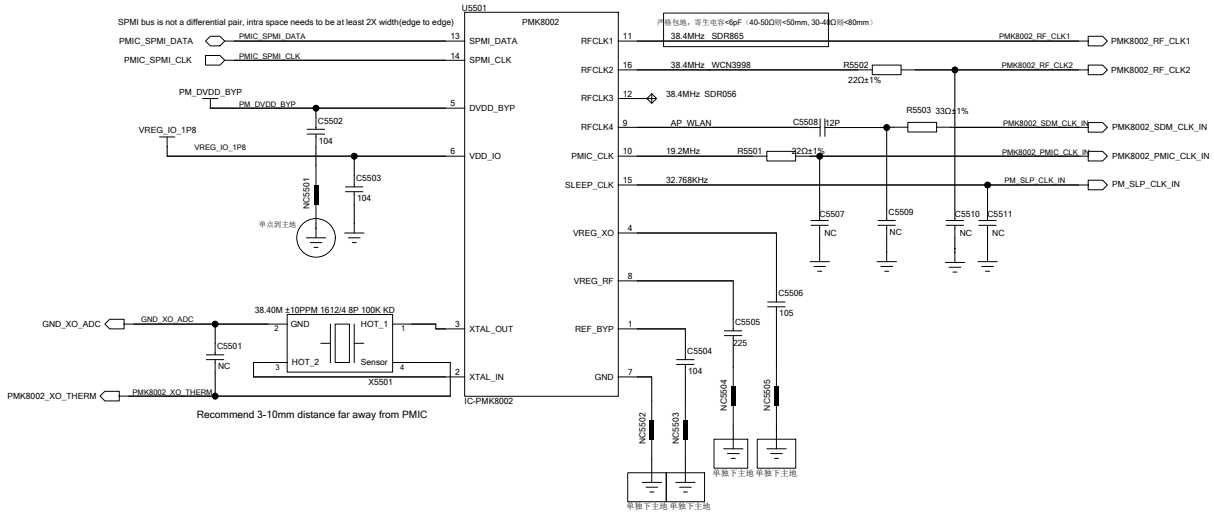
PMK8002



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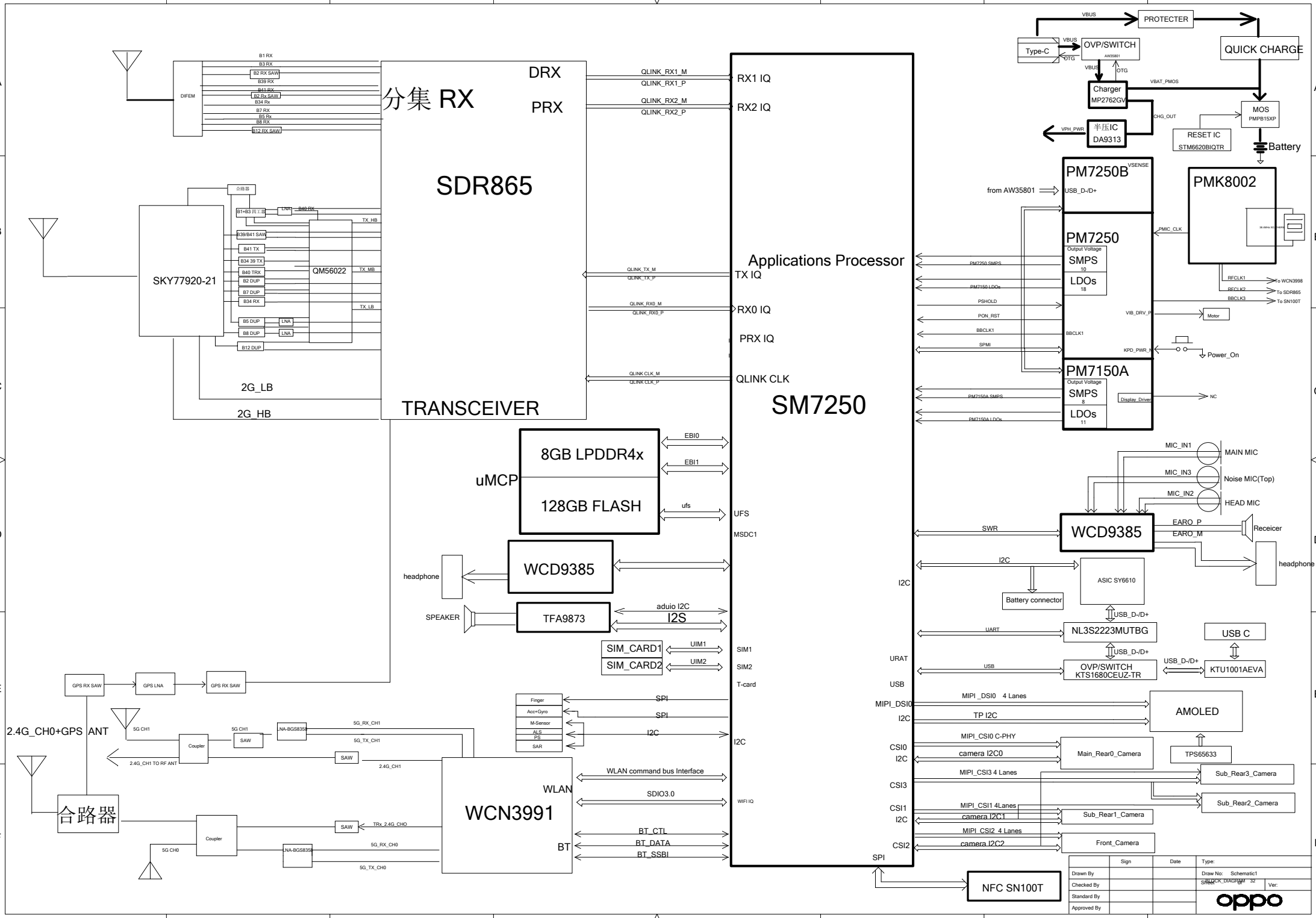
分集 RX
DRX
PRX
SDR865
TRANSCEIVER
DIFEM
B1 RX
B3 RX
B2 RX SAW
B39 RX
B41 RX
B2 Rx SAW
B34 Rx
B7 RX
B5 Rx
B8 RX
B12 RX SAW
SKY77920-21
合路器
B1+B3 四工器
LNA
B40 RX
B39/B41 SAW
B41 TX
B34 39 TX
B40 TRX
B2 DUP
B7 DUP
B34 RX
B5 DUP
B8 DUP
B12 DUP
QM56022
TX_HB
TX_MB
TX_LB
2G_LB
2G_HB
QLINK_RX1_M
QLINK_RX1_P
QLINK_RX2_M
QLINK_RX2_P
QLINK_TX_M
QLINK_TX_P
QLINK_RX0_M
QLINK_RX0_P
QLINK CLK_M
QLINK CLK_P
RX1 IQ
RX2 IQ
Applications Processor
TX IQ
RX0 IQ
PRX IQ
QLINK CLK
SM7250
8GB LPDDR4x
128GB FLASH
uMCP
EBI0
EBI1
ufs
UFS
MSDC1
headphone
WCD9385
SPEAKER
TFA9873
aduio I2C
I2S
SIM_CARD1
SIM_CARD2
UIM1
UIM2
SIM1
SIM2
T-card
GPS RX SAW
GPS LNA
GPS RX SAW
2.4G_CH0+GPS ANT
5G CH1
Coupler
SAW
LNA-BGS8358
5G_RX_CH1
5G_TX_CH1
2.4G_CH1 TO RF ANT
2.4G_CH1
合路器
5G CH0
TRx_2.4G_CH0
5G_RX_CH0
5G_TX_CH0
WCN3991
WLAN
BT
Finger
Acc+Gyro
M-Sensor
ALS
PS
SAR
SPI
I2C
WLAN command bus Interface
SDIO3.0
WIFI IQ
BT_CTL
BT_DATA
BT_SSBI
VBUS
PROTECTER
Type-C
OTG
OVP/SWITCH
AW35801
QUICK CHARGE
Charger
MP2762GV
VBAT_PMOS
CHG_OUT
MOS
PMPB15XP
VPH_PWR
半压IC
DA9313
RESET IC
STM6620BIQTR
Battery
PM7250B
VSENSE
USB_D-/D+
from AW35801
PMK8002
PM7250
Output Voltage
SMPS
10
LDOs
18
PMIC_CLK
PM7250 SMPS
PM7250 LDOs
PSHOLD
PON_RST
BBCLK1
SPMI
RFCLK1
RFCLK2
BBCLK3
To WCN3998
To SDR865
To SN100T
VIB_DRV_P
Motor
KPD_PWR_N
Power_On
PM7150A
SMPS
8
LDOs
11
PM7150A SMPS
PM7150A LDOs
Display_Driver
NC
MIC_IN1
MIC_IN3
MIC_IN2
MAIN MIC
Noise MIC(Top)
HEAD MIC
SWR
WCD9385
EARO_P
EARO_M
Receicer
headphone
I2C
ASIC SY6610
Battery connector
USB_D-/D+
UART
NL3S2223MUTBG
USB C
URAT
USB
OVP/SWITCH
KTS1680CEUZ-TR
KTU1001AEVA
MIPI _DSI0 4 Lanes
TP I2C
AMOLED
TPS65633
MIPI_CSI0 C-PHY
camera I2C0
Main_Rear0_Camera
MIPI_CSI3 4 Lanes
Sub_Rear3_Camera
Sub_Rear2_Camera
MIPI_CSI1 4Lanes
camera I2C1
Sub_Rear1_Camera
MIPI_CSI2 4 Lanes
camera I2C2
Front_Camera
NFC SN100T
Sign
Date
Type:
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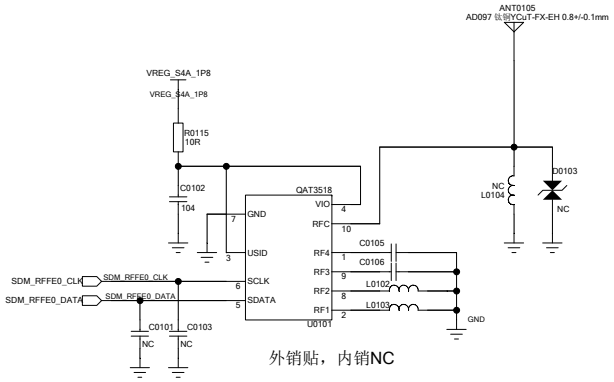
Checked By
Standard By
Approved By
Draw No: Schematic1
Sheet 1 of 32
Ver:
BLOCK DIAGRAM
oppo

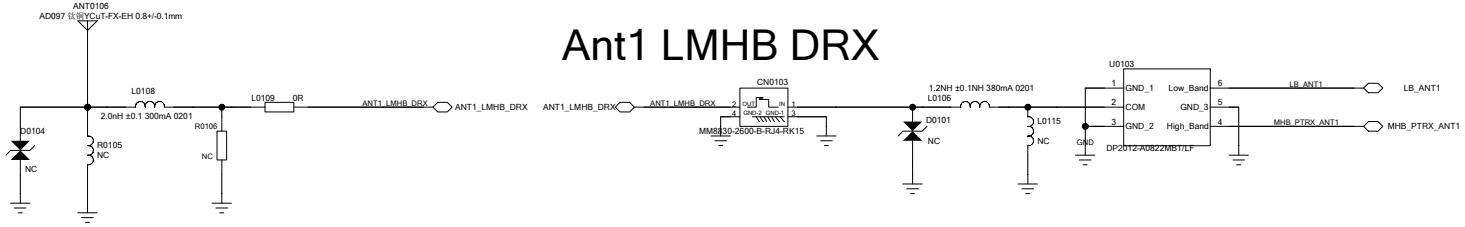
Ant1 LMHB DRX



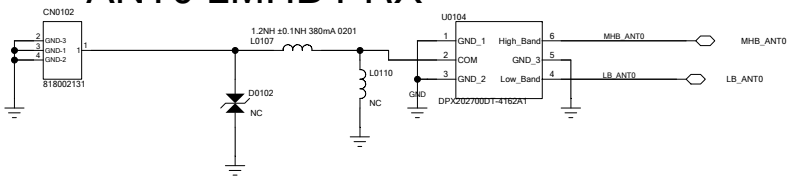
外销贴，内销NC

Connect to Vio	0	0110
Connect to GND	1	0111

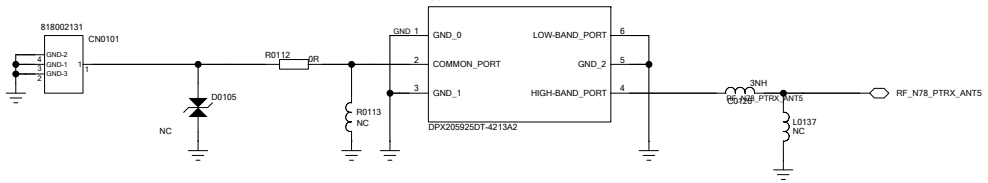
上天线 右侧



ANT0 LMHB PRX

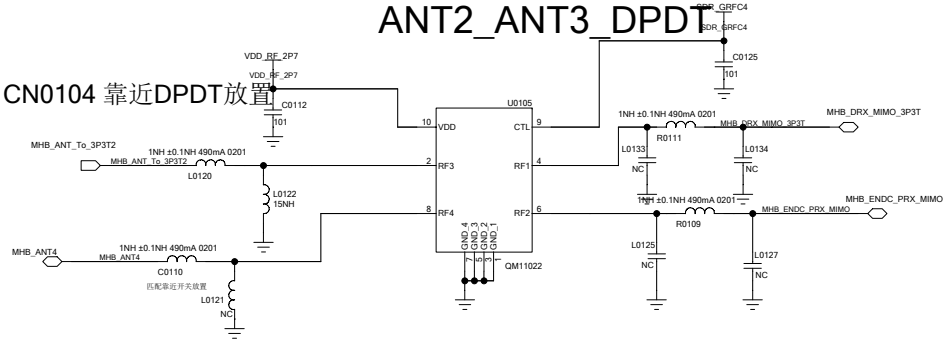


Ant5 MHB MIMO PRX+N41/78/79 MIMO DRX

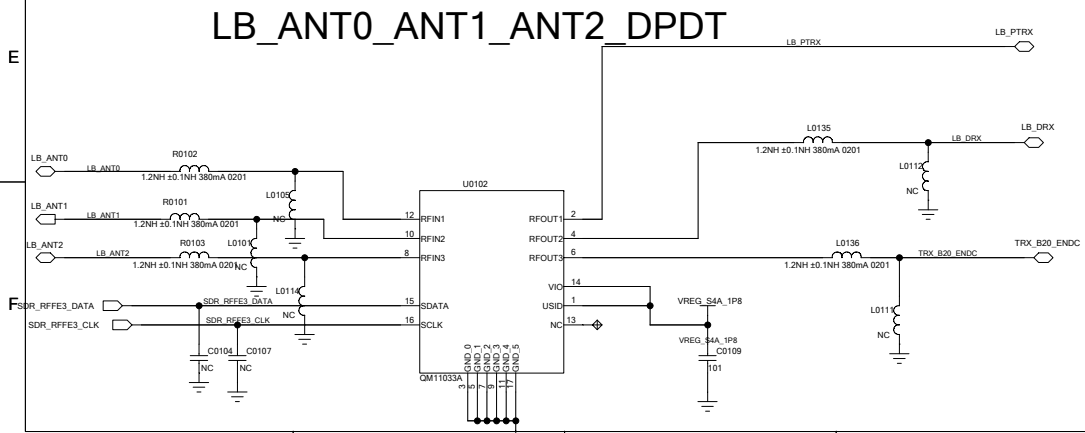


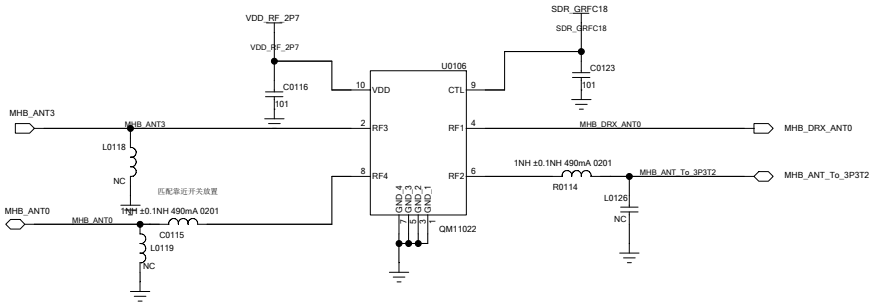
ANT2_ANT3_DPDT

CN0104 靠近DPDT放置



LB_ANT0_ANT1_ANT2_DPDT





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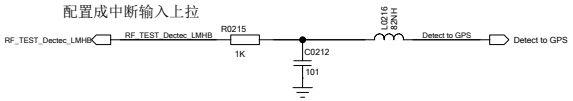
Approved By			

oppo

Connect to GND	1010

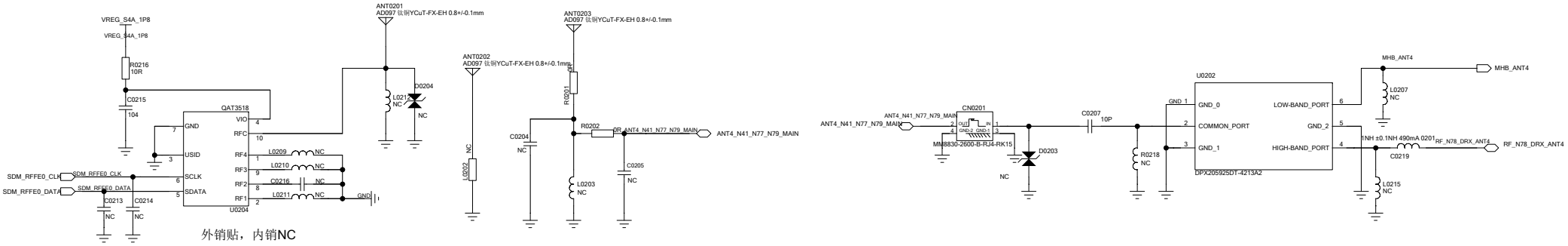
平台没有内置2.8V LDO，使用外置LDO供电

配置成中断输入上拉



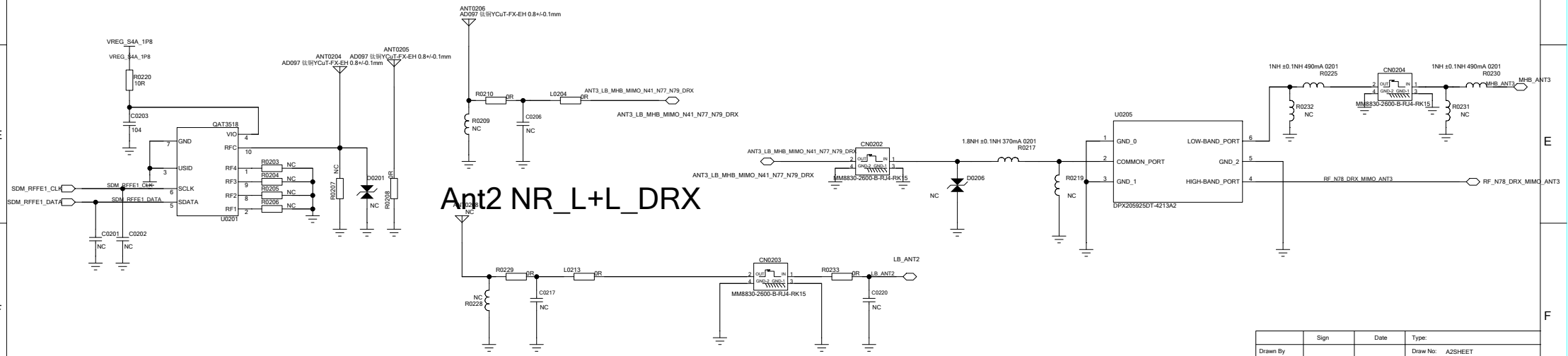
压板传导测试检测电路

Ant4 N78/N79 PRX/NR_MHB PRX



外销贴，内销NC

Ant3 MHB MIMO2+ N78/79 MIMO3



Ant2 NR_L+L_DRX

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Checked By			Sheet of 47	Ver:
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Approved By				

LB Pamid

衰减匹配网络值待确定！要考虑GSM和HPUE

LTE_LMHB_FBRX_OUT — 18R L0501 — 6dB — 18R L0502 — C0513 68R

FBRX_MHB_OUT — QM77048 PA输出匹配，靠近QM77043摆放 — 0R R0518 — C0538 NC — C0539 NC

QM77048 开关端口匹配，靠近QM77048摆放 — R0515 1.5NH ±0.1NH 420mA 0201 — R0514 1P — R0516 NC — GSM_HB_OUT

VPA_2G_VCC — C0509 225 — C0511 NC — C0512 101

VPH_PWR — C0515 102 — C0516 475

SDR_RFFE1_CLK — SDR_RFFE1_CLK — C0503 NC — C0506 NC

SDR_RFFE1_DATA — SDR_RFFE1_DATA

VREG_S4A_1P8 — VREG_S4A_1P8 — C0507 102

SDR_TX0_GSM_MB — SDR_TX0_GSM_MB — R0504 0R — R0502 NC — R0506 NC

SDR_TX0_GSM_LB — SDR_TX0_GSM_LB — L0508 0R — L0512 15NH — L0513 15NH

SDR_TX0_34G_LB — SDR_TX0_34G_LB — R0505 0R — R0507 NC

VPA_4G_LMHB — VPA_4G_LMHB — R0511 0R — 200mA — VCC1 — VCC2 — 800mA — 1000mA

C0502 NC — C0505 NC — C0508 NC — C0510 NC

兼容SKYS8081 — 0R R0517 — LB_PTRX — C0517 NC — LB_PTRX C0526 NC

U0501 — QM77043

外销使用QM77043

2G_VCC_2 — 2G_VCC_1 — VBAT — VRAMP — GND_7 — GND_6 — GND_5 — GND_4 — 2GHB_TXOUT — GND_3 — CPL_IN — CPL_OUT — GND_2 — NC_0 — ANT_LB

GND_9 — SCLK1 — SDATA1 — VIO1 — GND_10 — MB_IN — LB_IN — LB_IN_4G — GND_11 — GND_12 — GND_13 — 3G4G_VCC1 — GND_14

3G4G_VCC2 — GND_15 — LB_TXOUT4 — LB_TXOUT3 — LB_TXOUT2 — LB_TXOUT1 — GND_16 — SCLK2 — SDATA2 — VIO2 — LNA_VDD — GND_17 — LNA_OUT1 — LNA_OUT2 — LNA_OUT3

GND_0 — GND — LB_TRX1 — LB_TRX2 — LB_TRX3 — LB_TRX4 — GND_21 — LNA_AUX1 — LNA_AUX2 — LNA_AUX3 — LNA_AUX4 — GND_20 — NC_1 — GND_18

TRX_B28B — TRX_B28A

PRX_LNA_B20_ENDC — C0533 50V 47P — C0534 50V 47P — L0504 50V 47P — 3.3NH ±0.3NH L0505 — L0506 50V 47P — L0507 50V 47P — PRX_LNA_B28A — PRX_LNA_B28B

C0521 NC — C0524 NC — C0535 NC — C0537 NC — C0536 NC

SDR_PRX10 — SDR_PRX6

VREG_L6A_1P20_RF — C0531 101 — C0532 104 — VREG_S4A_1P8 — C0529 102

SDR_RFFE7_DATA — SDR_RFFE7_CLK — TX_RF_OUT_B28A — TX_RF_OUT_B28B

B28A TRX

TX_RF_OUT_B28A — C0520 2.0nH ±0.1 300mA 0201 — L0514 NC — L0515 18NH

Close to PA

B28A更换为9040321隔离度更好

B39771B1252P810 — Z0502 — TX — RX — ANT — GND_4 — GND_3 — GND_2 — GND_1 — GND_0 — PRX_LNA_B28A

TRX_B28A — L0516 0R — C0519 NC — L0519 5.6NH

B28B TRX

Close to PA

TX_RF_OUT_B28B — C0501 10P — L0517 NC — L0518 5.6NH

TRX_B28B — L0520 1NH ±0.1NH 490mA 0201 — L0521 NC — L0522 5.6NH

Z0501 — TX — RX — ANT — GND_4 — GND_3 — GND_2 — GND_1 — GND_0 — B1253 — PRX_LNA_B28B

	Sign	Date	Type:
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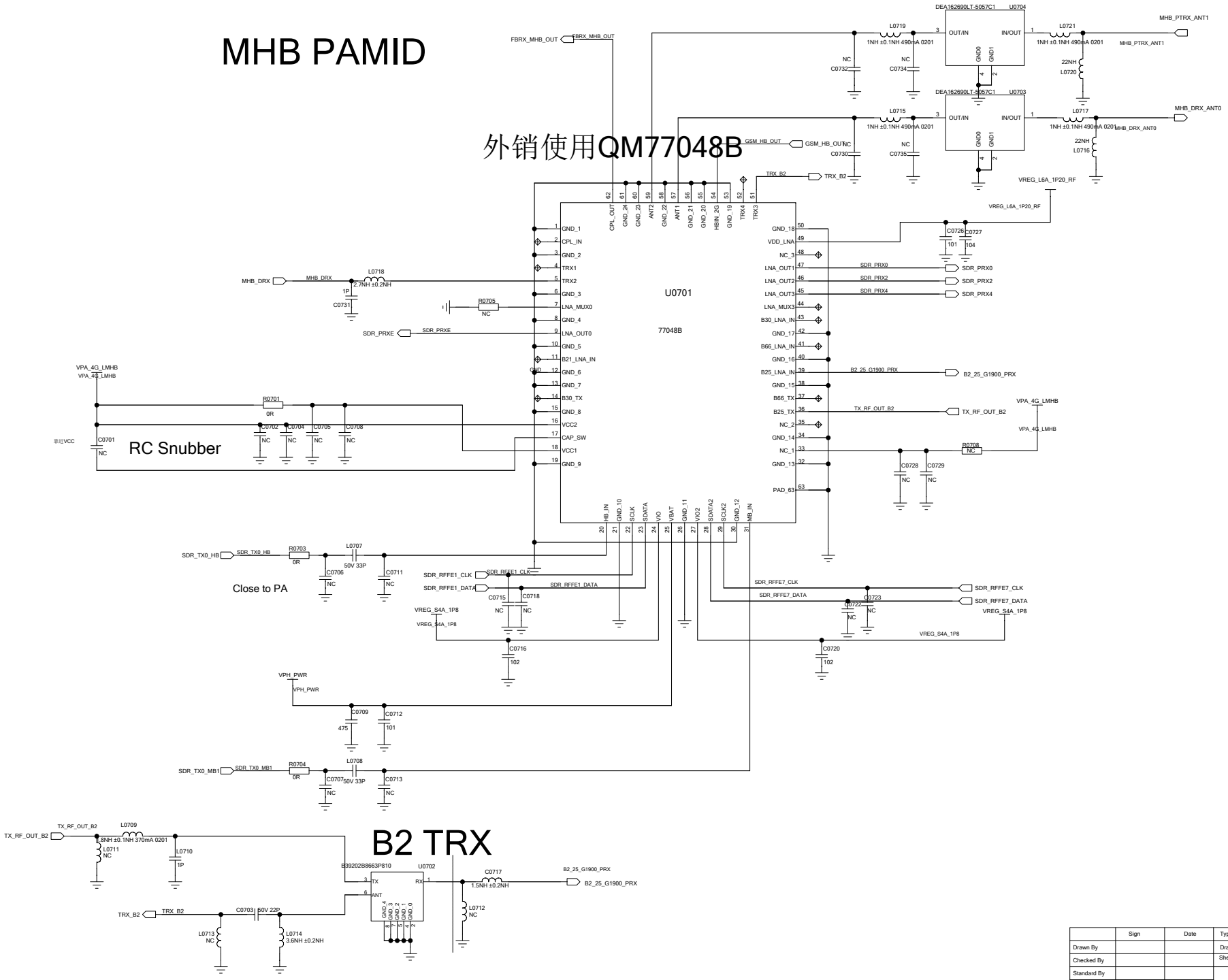
Approved By			

MHB PAMID

外销使用QM77048B



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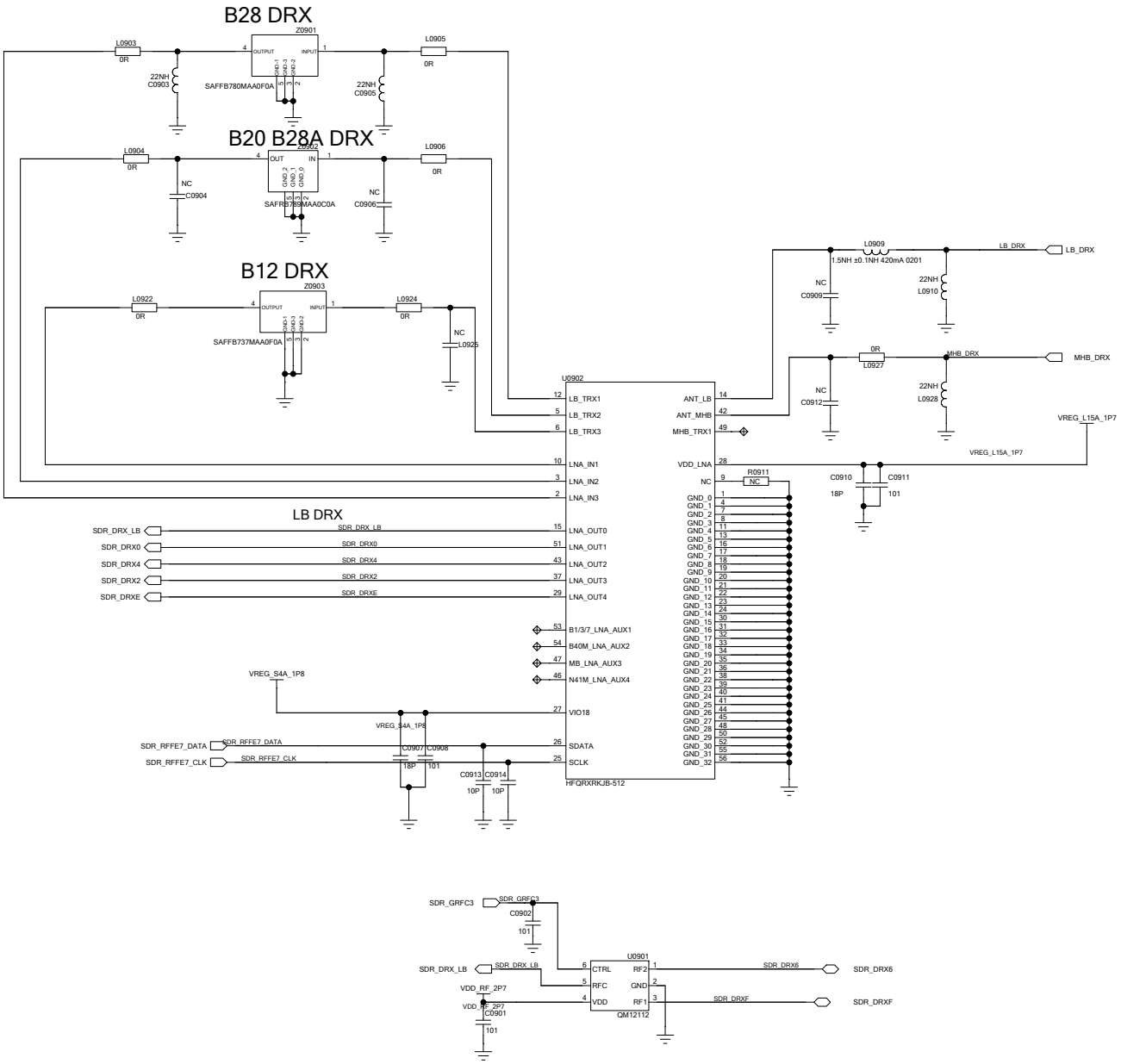
7_2/3/4G PTRX_MHB_PAMID_QM77048B

DRX Module



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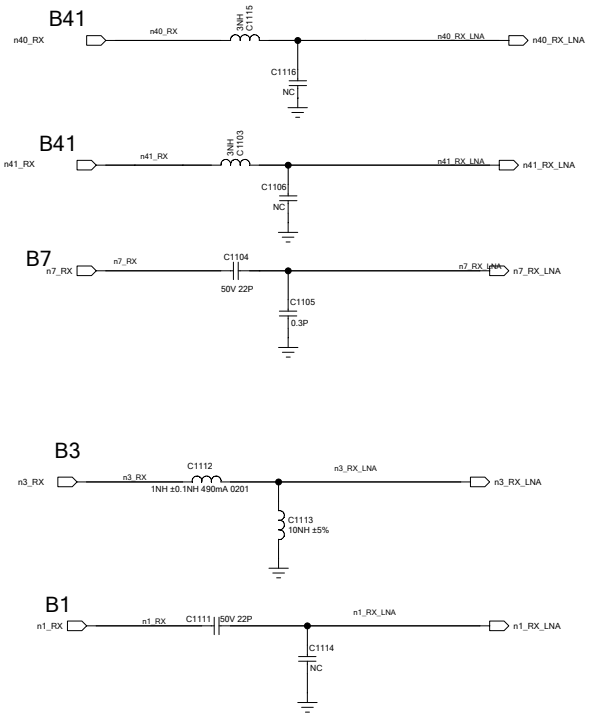
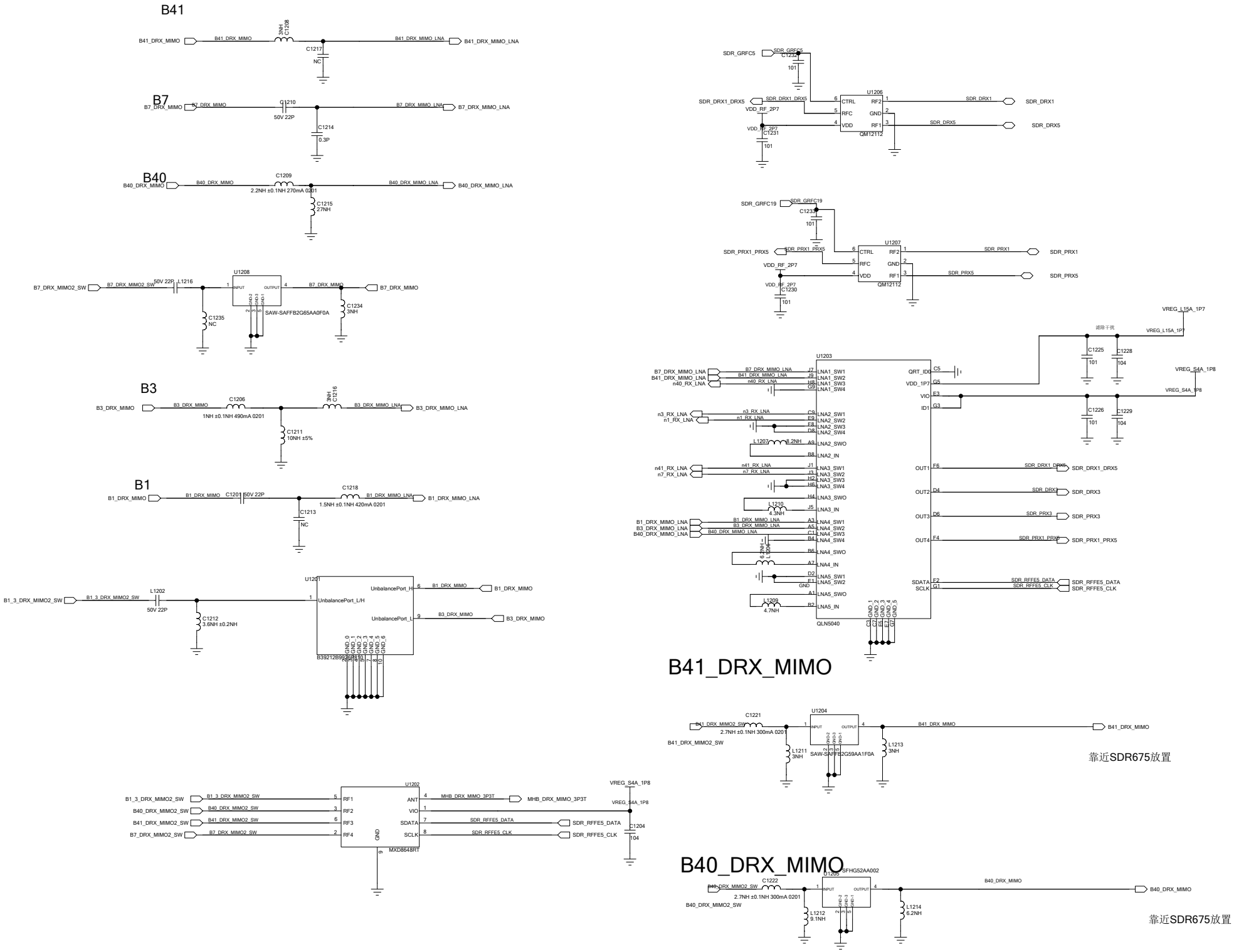

B41
n40_RX
n40_RX
2NH
C1115
n40_RX_LNA
n40_RX_LNA
C1116
NC
B41
n41_RX
n41_RX
2NH
C1103
n41_RX_LNA
n41_RX_LNA
C1106
NC
B7
n7_RX
n7_RX
C1104
50V 22P
n7_RX_LNA
n7_RX_LNA
C1105
0.3P
B3
n3_RX
n3_RX
C1112
1NH ±0.1NH 490mA 0201
n3_RX_LNA
n3_RX_LNA
C1113
10NH ±5%
B1
n1_RX
n1_RX
C1111
50V 22P
n1_RX_LNA
n1_RX_LNA
C1114
NC


B41
B41_DRX_MIMO
B41_DRX_MIMO
3NH C1208
B41_DRX_MIMO_LNA
B41_DRX_MIMO_LNA
C1217 NC
B7
B7_DRX_MIMO
B7_DRX_MIMO
C1210 50V 22P
B7_DRX_MIMO_LNA
B7_DRX_MIMO_LNA
C1214 0.3P
B40
B40_DRX_MIMO
B40_DRX_MIMO
C1209 2.2NH ±0.1NH 270mA 0201
B40_DRX_MIMO_LNA
B40_DRX_MIMO_LNA
C1215 27NH
B7_DRX_MIMO2_SW
B7_DRX_MIMO2_SW
50V 22P
L1216
U1208
INPUT
OUTPUT
B7_DRX_MIMO
B7_DRX_MIMO
C1235 NC
SAW-SAFFB2G65AA0F0A
C1234 3NH
B3
B3_DRX_MIMO
B3_DRX_MIMO
C1206 1NH ±0.1NH 490mA 0201
3NH C1216
B3_DRX_MIMO_LNA
B3_DRX_MIMO_LNA
C1211 10NH ±5%
B1
B1_DRX_MIMO
B1_DRX_MIMO
C1201 50V 22P
C1218 1.5NH ±0.1NH 420mA 0201
B1_DRX_MIMO_LNA
B1_DRX_MIMO_LNA
C1213 NC
B1_3_DRX_MIMO2_SW
B1_3_DRX_MIMO2_SW
L1202 50V 22P
C1212 3.6NH ±0.2NH
U1201
UnbalancePort_H
UnbalancePort_L/H
UnbalancePort_L
B39212B9224B810
B1_DRX_MIMO
B1_DRX_MIMO
B3_DRX_MIMO
B3_DRX_MIMO
B1_3_DRX_MIMO2_SW
B40_DRX_MIMO2_SW
B41_DRX_MIMO2_SW
B7_DRX_MIMO2_SW
U1202
RF1
RF2
RF3
RF4
ANT
VIO
SDATA
SCLK
GND
MXD8648RT
MHB_DRX_MIMO_3P3T
MHB_DRX_MIMO_3P3T
SDR_RFFE5_DATA
SDR_RFFE5_DATA
SDR_RFFE5_CLK
SDR_RFFE5_CLK
VREG_S4A_1P8
VREG_S4A_1P8
C1204 104
SDR_GRFC5
SDR_GRFC5
C1232 101
SDR_DRX1_DRX5
SDR_DRX1_DRX5
VDD_RF_2P7
VDD_RF_2P7
C1231 101
U1206
CTRL
RFC
VDD
RF2
GND
RF1
QM12112
SDR_DRX1
SDR_DRX1
SDR_DRX5
SDR_DRX5
SDR_GRFC19
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C1233 101
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SDR_PRX1_PRX5
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VDD_RF_2P7
C1230 101
U1207
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GND
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SDR_PRX1
SDR_PRX5
SDR_PRX5
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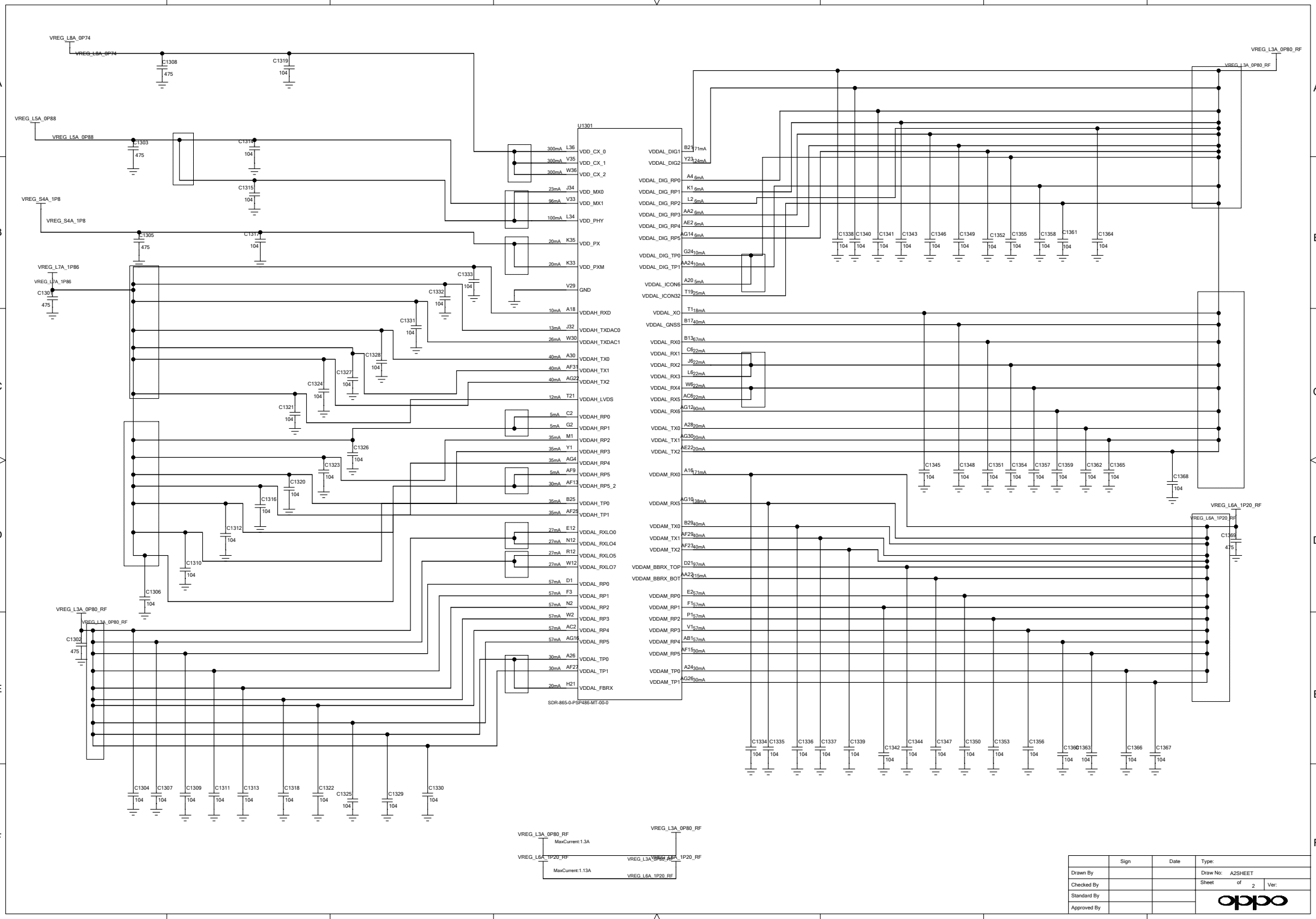
滤除干扰
C1225 101
C1228 104
VREG_S4A_1P8
VREG_S4A_1P8
C1226 101
C1229 104
U1203
B7_DRX_MIMO_LNA
B41_DRX_MIMO_LNA
n40_RX_LNA
B7_DRX_MIMO_LNA
B41_DRX_MIMO_LNA
n40_RX_LNA
J7 LNA1_SW1
J9 LNA1_SW2
H8 LNA1_SW3
G9 LNA1_SW4
n3_RX_LNA
n1_RX_LNA
n3_RX_LNA
n1_RX_LNA
C9 LNA2_SW1
E9 LNA2_SW2
F8 LNA2_SW3
D8 LNA2_SW4
L1207 6.2NH
A9 LNA2_SWO
B8 LNA2_IN
n41_RX_LNA
n7_RX_LNA
n41_RX_LNA
n7_RX_LNA
J1 LNA3_SW1
J3 LNA3_SW2
H2 LNA3_SW3
H6 LNA3_SW4
H4 LNA3_SWO
L1210 4.3NH
J5 LNA3_IN
B1_DRX_MIMO_LNA
B3_DRX_MIMO_LNA
B40_DRX_MIMO_LNA
B1_DRX_MIMO_LNA
B3_DRX_MIMO_LNA
B40_DRX_MIMO_LNA
A3 LNA4_SW1
A5 LNA4_SW2
C1 LNA4_SW3
B4 LNA4_SW4
L1206 6.2NH
B6 LNA4_SWO
A7 LNA4_IN
D2 LNA5_SW1
E1 LNA5_SW2
GND
A1 LNA5_SWO
L1209 4.7NH
B2 LNA5_IN
QLN5040
QRT_IDC
VDD_1P7
VIO
ID1
C5
G5
E3
G3
OUT1
OUT2
OUT3
OUT4
SDATA
SCLK
F6
D4
D6
F4
F2
G1
SDR_DRX1_DRX5
SDR_DRX1_DRX5
SDR_DRX3
SDR_DRX3
SDR_PRX3
SDR_PRX3
SDR_PRX1_PRX5
SDR_PRX1_PRX5
SDR_RFFE5_DATA
SDR_RFFE5_CLK
SDR_RFFE5_DATA
SDR_RFFE5_CLK
C3 GND_1
C2 GND_2
E5 GND_3
E7 GND_4
G7 GND_5
B41_DRX_MIMO
C1221 2.7NH ±0.1NH 300mA 0201
B41_DRX_MIMO2_SW
B41_DRX_MIMO2_SW
U1204
INPUT
OUTPUT
SAW-SAFFB2G59AA1F0A
L1211 3NH
L1213 3NH
B41_DRX_MIMO
B41_DRX_MIMO
靠近SDR675放置
B40_DRX_MIMO
U1205 SFHG52AA002
B40_DRX_MIMO2_SW
B40_DRX_MIMO2_SW
C1222 2.7NH ±0.1NH 300mA 0201
INPUT
OUTPUT
L1212 9.1NH
L1214 6.2NH
B40_DRX_MIMO
B40_DRX_MIMO
靠近SDR675放置



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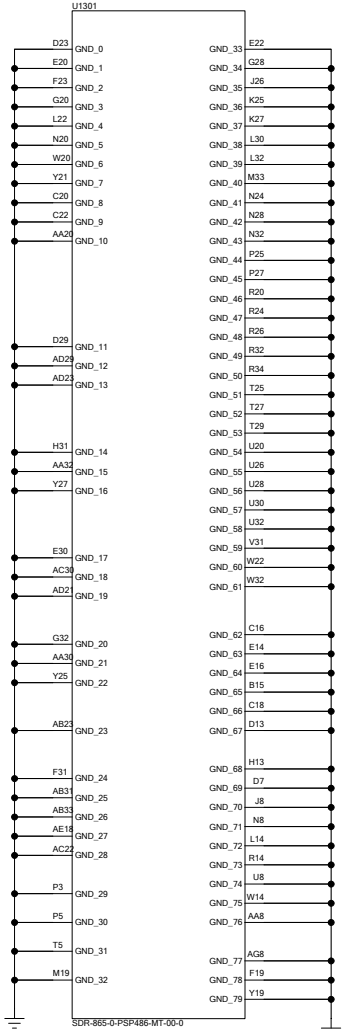
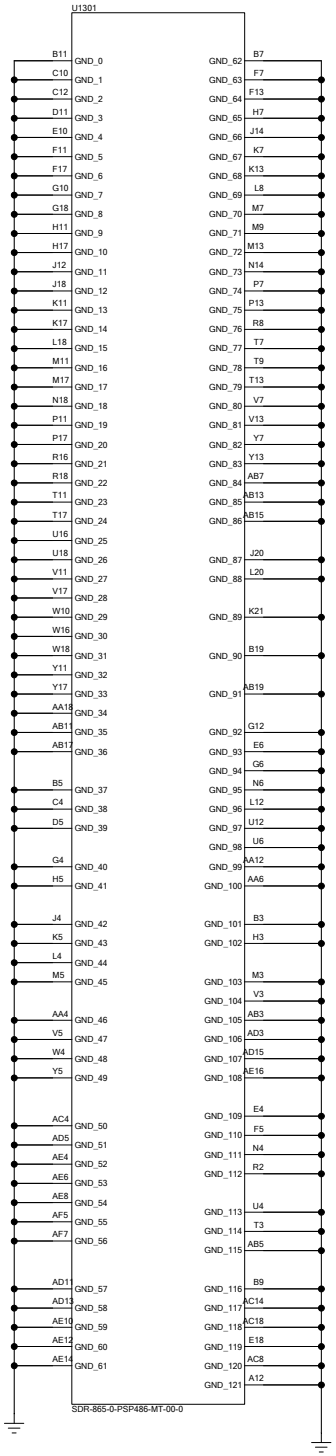
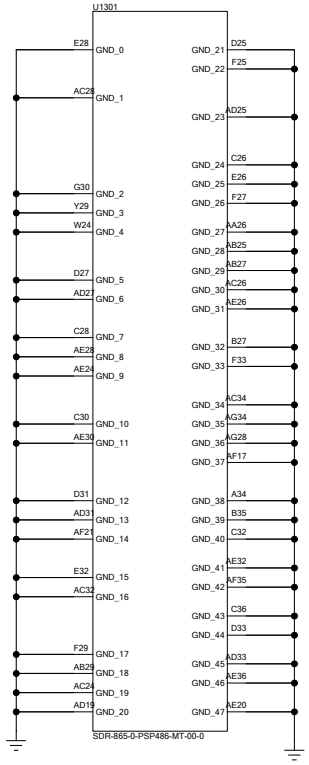
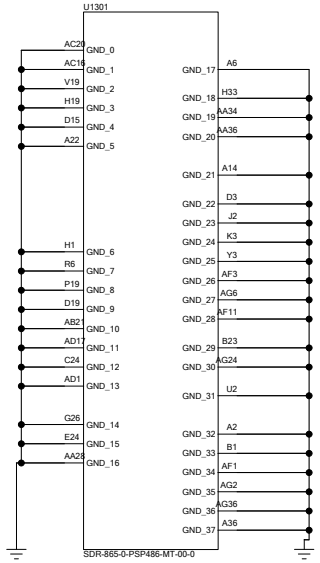
Approved By				







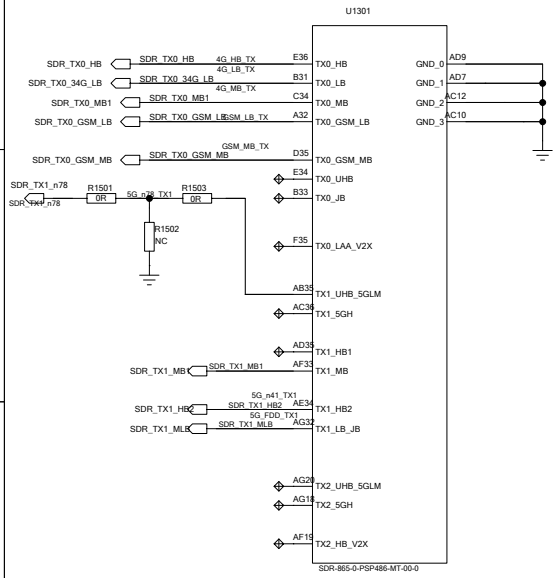


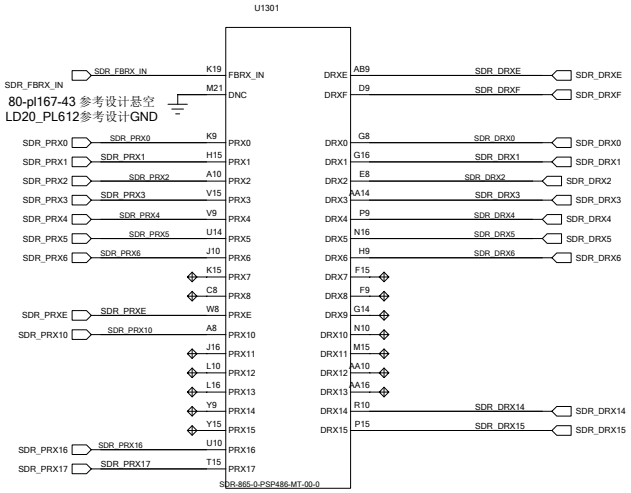
PDN Guidelines for LPDDR4X

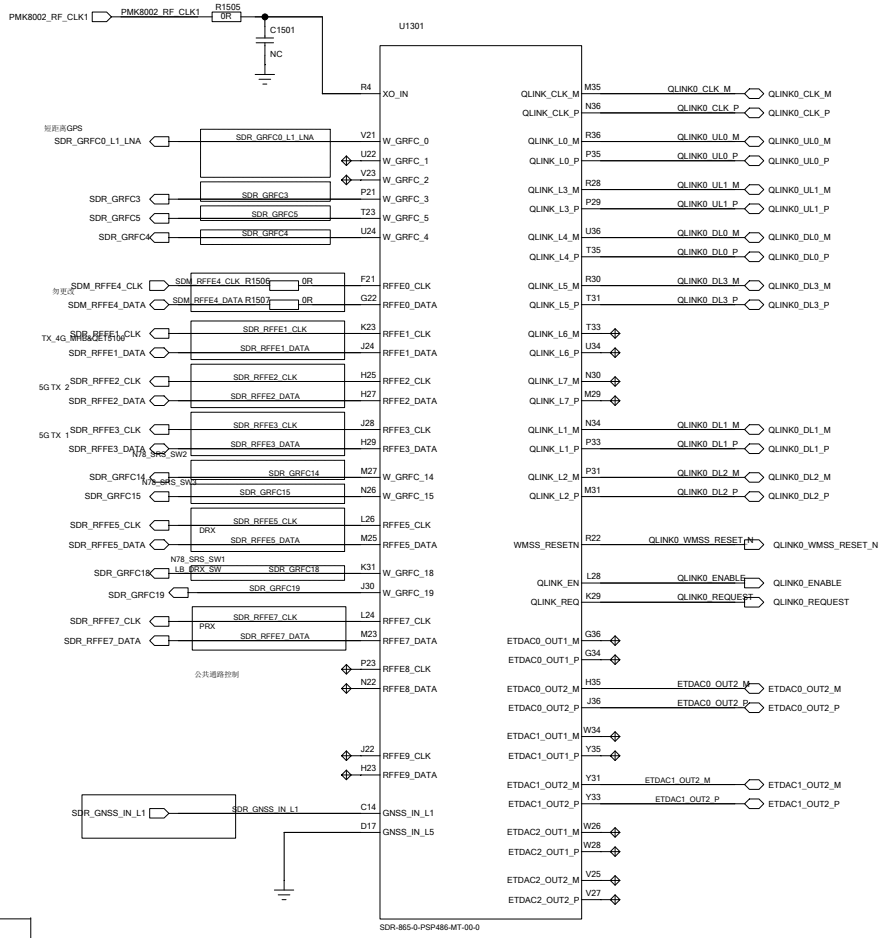
	(DC)	(AC+DC)	DC R	AC Z@20MHz	De-cap. Combination
VDDQ(0.6V)	±18mV	±30mV	<15mΩ	<38mΩ	Ch. A 2.2uF 1ea + 100nF 2ea Ch. B 2.2uF 1ea + 100nF 2ea
VDD2(1.1V)	±33mV	±55mV	<8mΩ	<38mΩ	Ch. A 4.7uF 1ea + 100nF 2ea Ch. B 4.7uF 1ea + 100nF 2ea
VDD1(1.8V)	±55mV	±90mV	<40mΩ	<126mΩ	(2.2uF + 100nF) * 2

	Sign	Date	Type:	
Drawn By			Draw No: A2SHEET	
Checked By			Sheet 2 of	Ver:
Standard By			oppo	
Approved By				

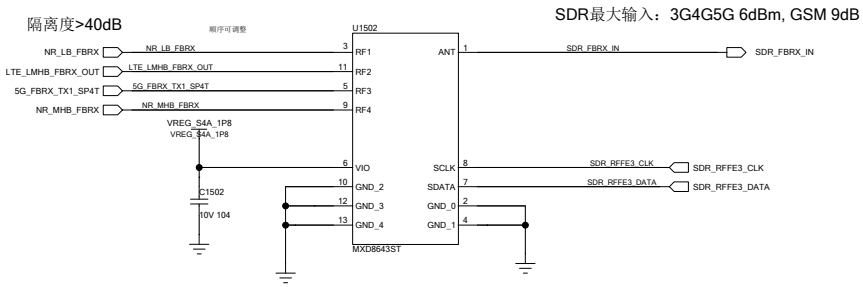
Page9_1_SDR_TX&RX







FBRX Switch



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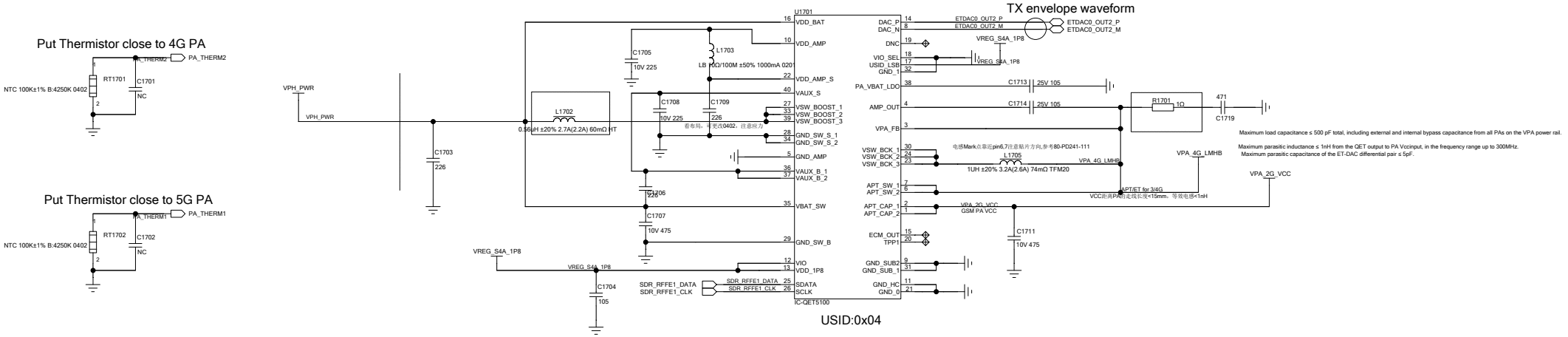
Checked By			Sheet of 2	Ver:
Standard By	Elvis	2014/01/15	Schematic1	
Approved By			11_SDR865_TX&RX_VMS32	

QET5100 #0 for 4G

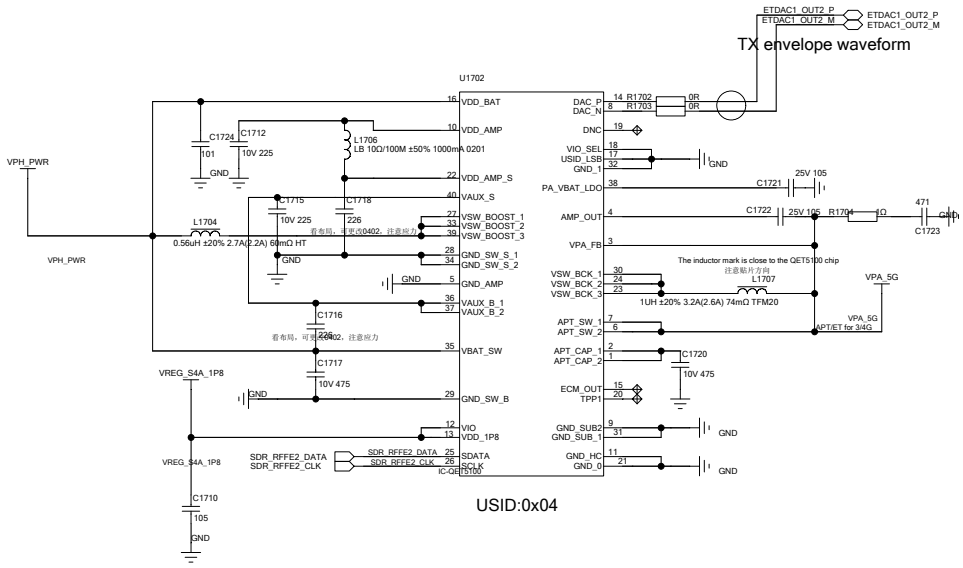
QET5100 #0 for QM77043&QM77048B



QET5100 #1 for 5G(外销)

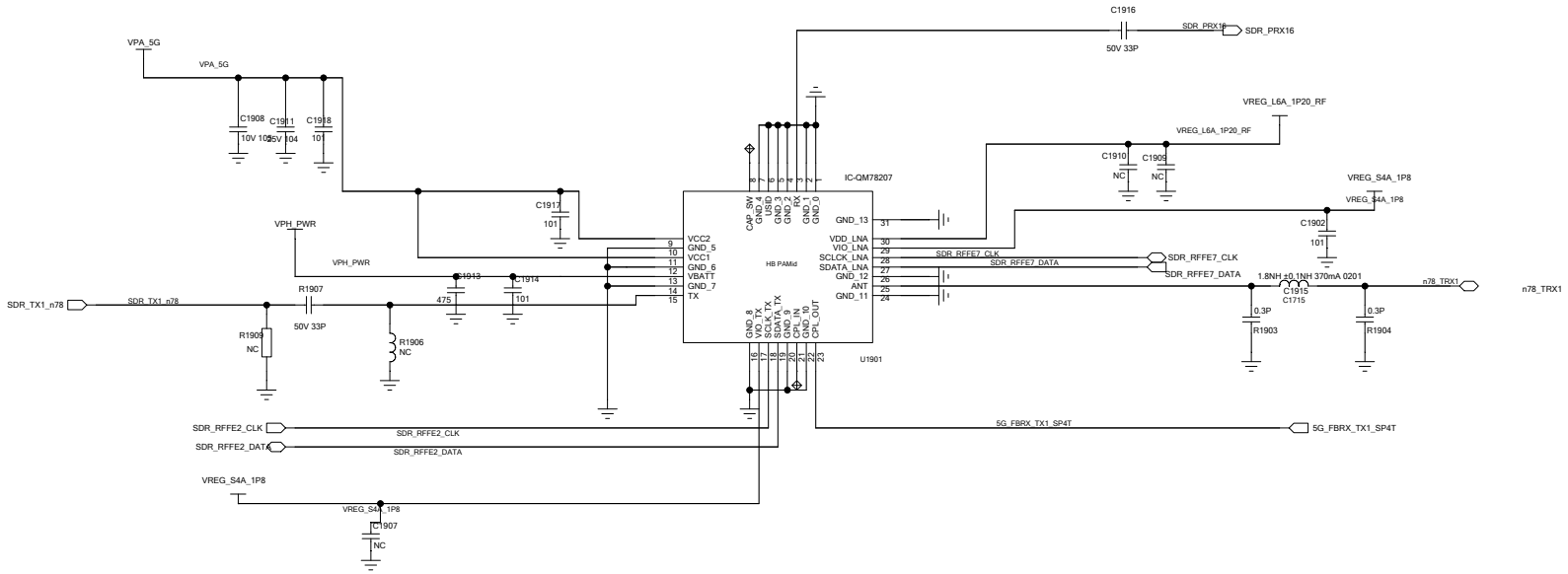
QET5100 #1 for QM78207&VC7643-63

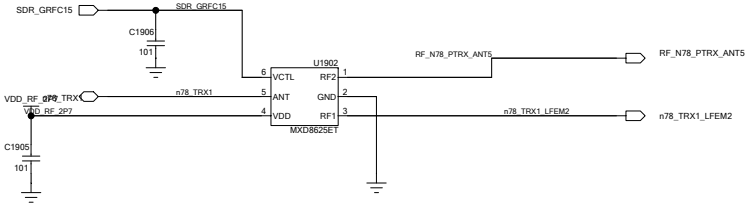
高通确认需要使用耐压值10V
9月30日可以选用9870022



	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet of 2	Ver:
Standard By			oppo	
Approved By				

#0(主通路) n78&N79_TX1





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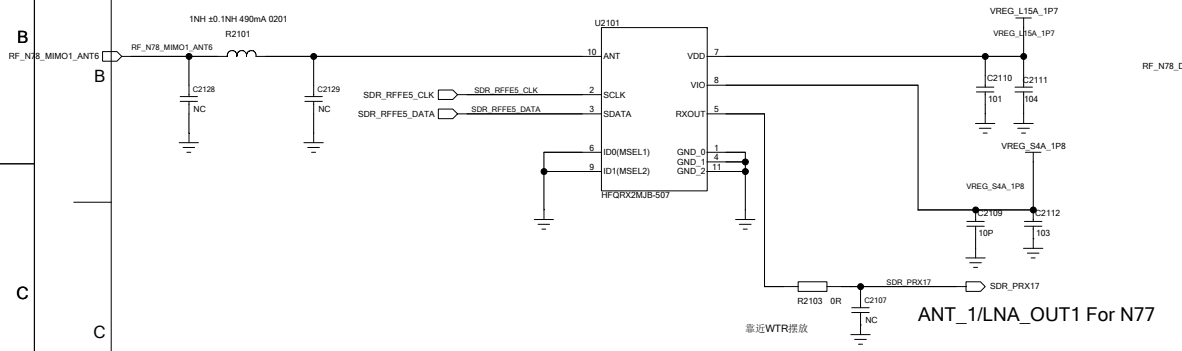
Checked By			Sheet of 52 Ver:
Standard By			
Approved By			

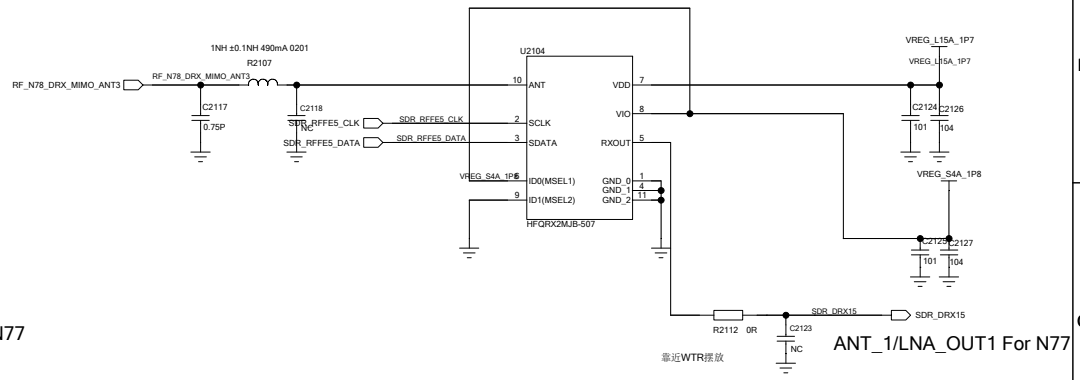
NR_LFEM_1



ANT_1/LNA_OUT1 For N77

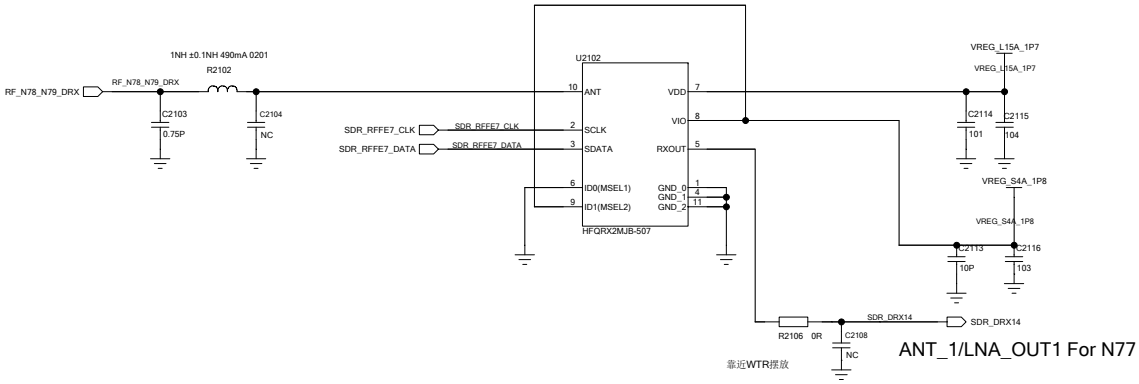
ID1	ID0	USID
GND	GND	0x07
GND	VIO	0x08
VIO	GND	0x09
VIO	VIO	0x0A

NR_LFEM_DRX_3

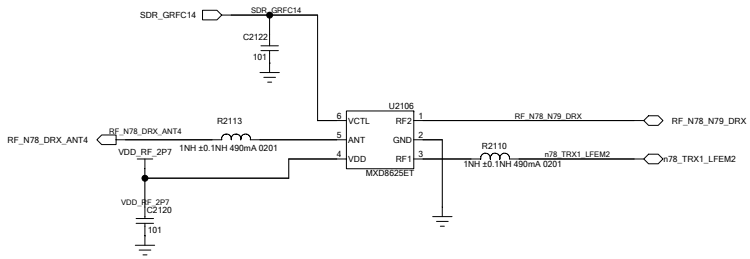


ANT_1/LNA_OUT1 For N77

NR_LFEM_2



ANT_1/LNA_OUT1 For N77



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Standard By	Drawn By			Drawing Schematic
Approved By	Checked By			62 Ver:
	Standard By			
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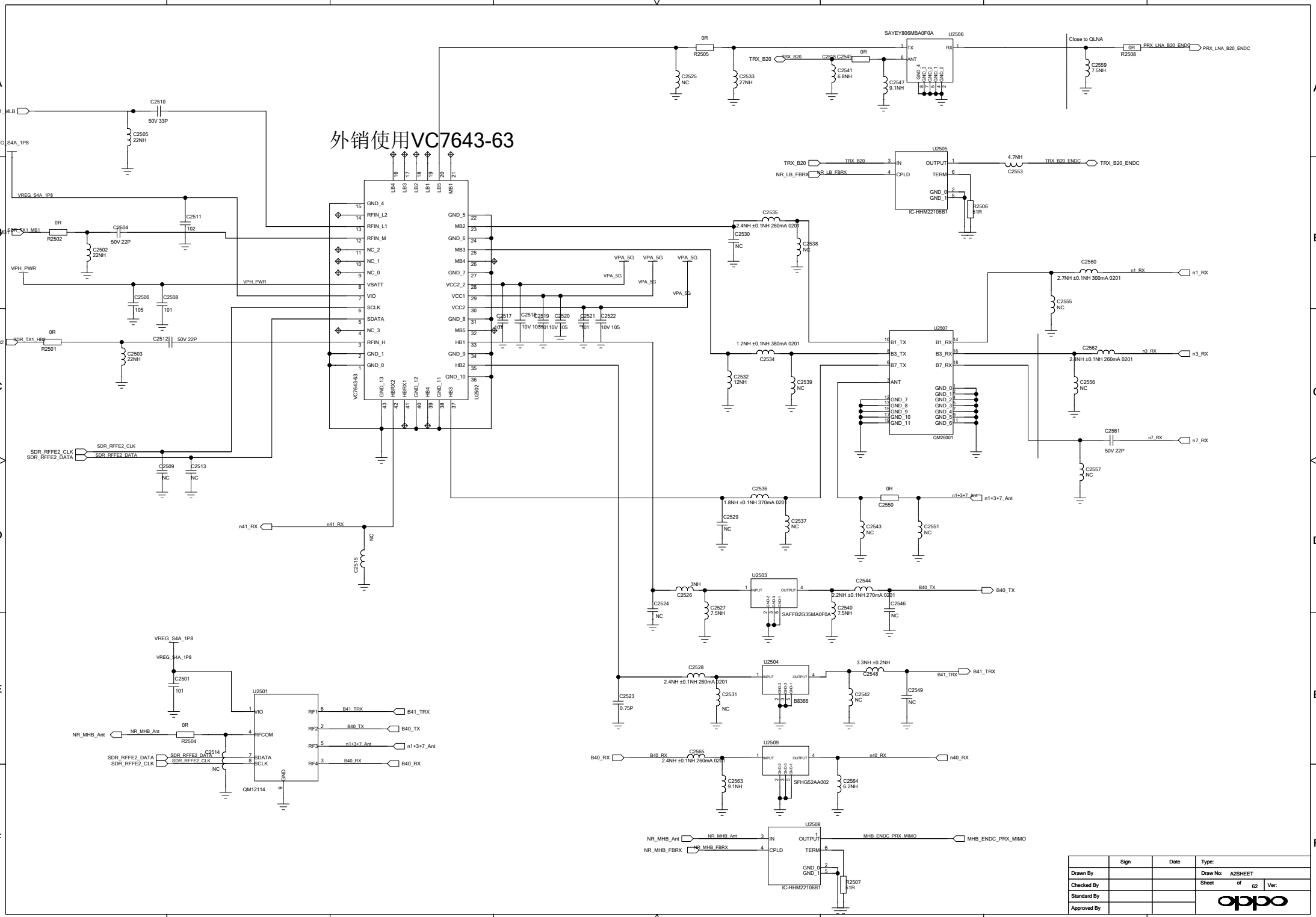

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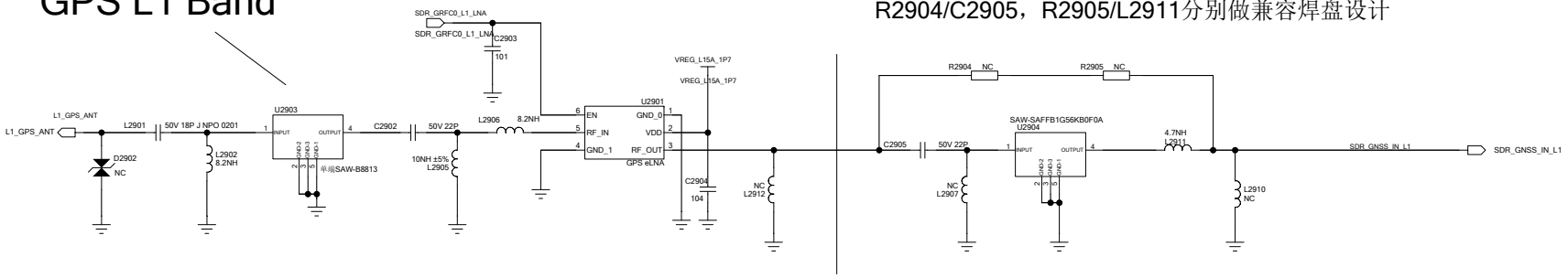
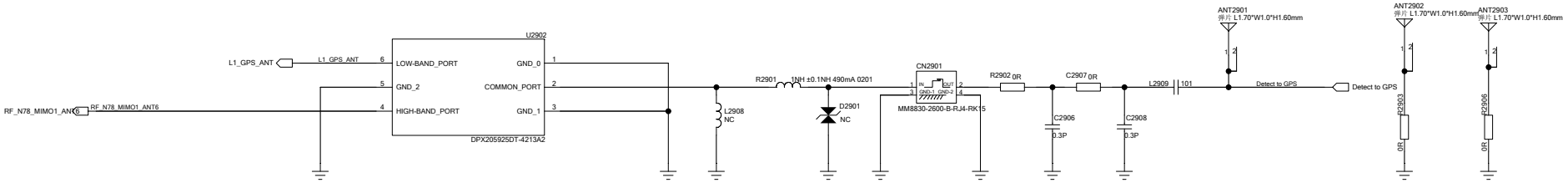
Drawn By			Draw No: A2SHEET	
Checked By			Sheet of 62	Ver:
Standard By				
Approved By				

GPS L1 Band

Close to SDR
R2904/C2905，R2905/L2911分别做兼容焊盘设计



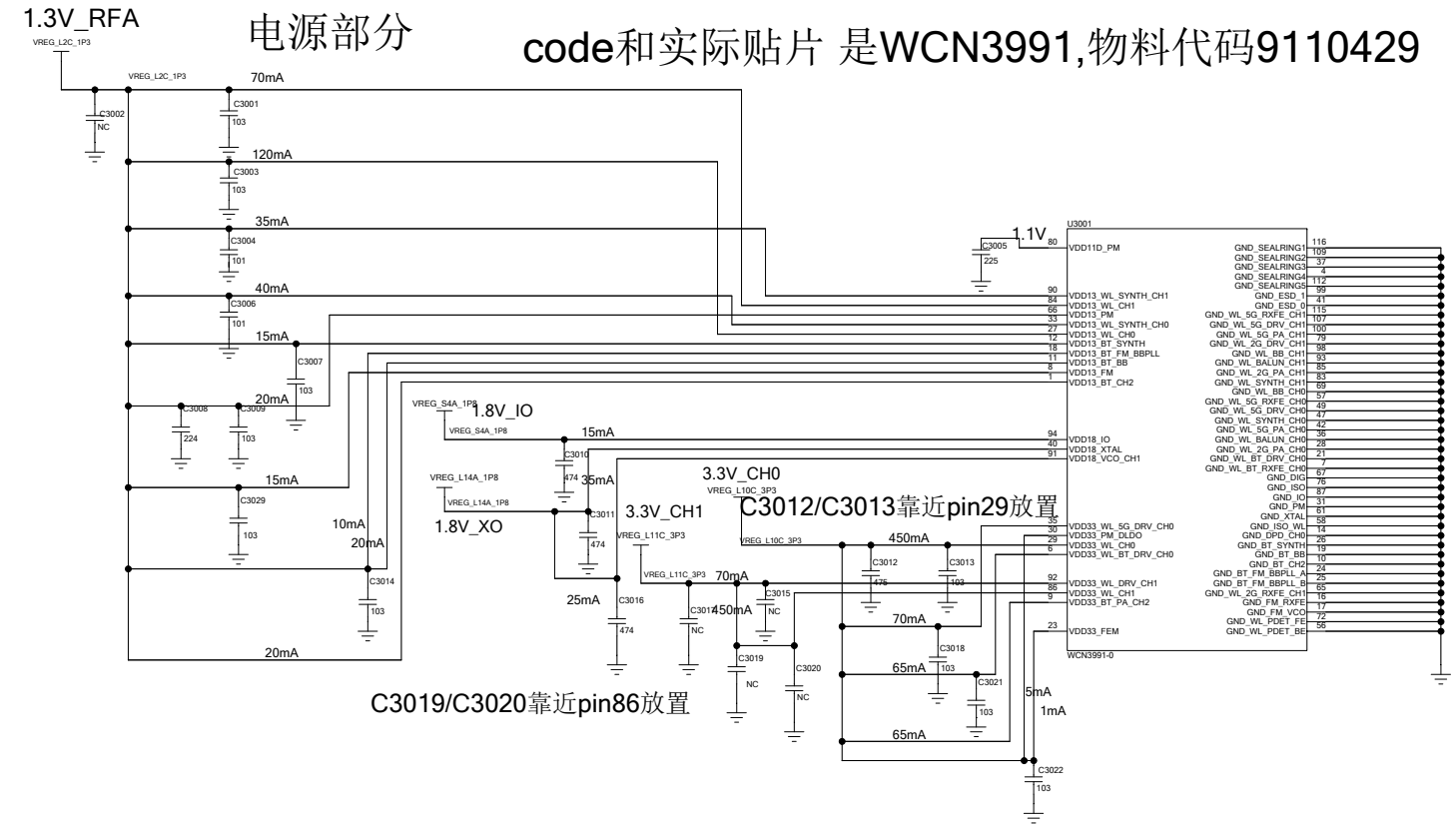
ANT6 GPS+N78 T/RX



	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet 12_RF of 32	Ver:
Standard By			oppo	
Approved By				

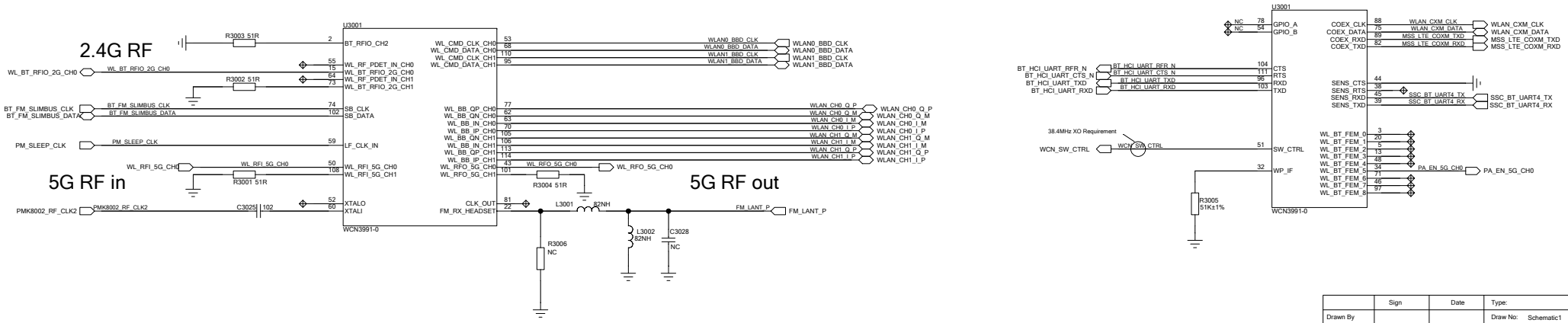
WCN3991
电源部分

code和实际贴片 是WCN3991,物料代码9110429



PIN脚名称	PIN脚	电流大小
VDD13_WL_CH0	27	120mA
VDD13_WL_CH1	84	70mA
VDD13_WL_SYNTH_CH0	33	35mA
VDD13_WL_SYNTH_CH1	90	40mA
VDD13_BT_SYNTH	12	15mA
VDD13_PM	66	20mA
VDD13_FM	8	15mA
VDD12_BT_FM_BBPLL	18	10mA
VDD13_BT	11	20mA
VDD13_BT_CH2	1	20mA
VDD33_WL_CH0	29	450mA
VDD33_WL_5GPA_DRV_CH0	35	70mA
VDD33_WL_BT_DRV_CH0	6	65mA
VDD33_BT_PA_CH2	9	65mA
VDD33_PM_DLDO	30	5mA
VDD33_FEM	23	1mA
VDD33_WL_CH1	86	450mA
VDD33_WL_5GPA_DRV_CH1	92	70mA
VDD18_IO	94	15mA
VDD18_XTAL	40	35mA
VDD18_VCO_CH1	91	25mA

WCN3991 Interface

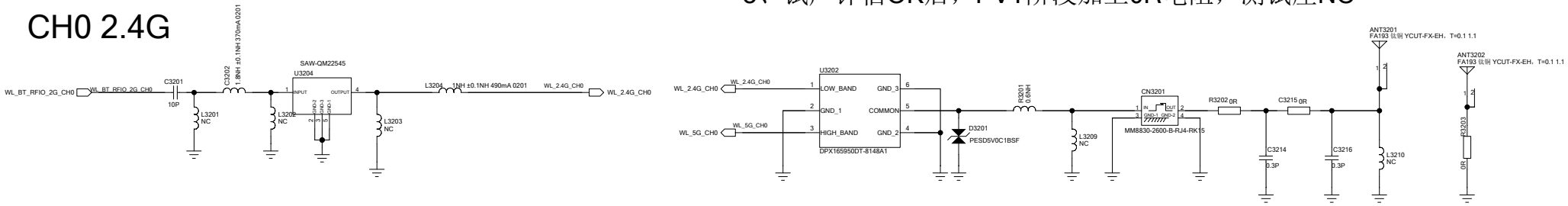


	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet WCN3990/PIB 32 of 32 Ver:
Standard By			oppo
Approved By			

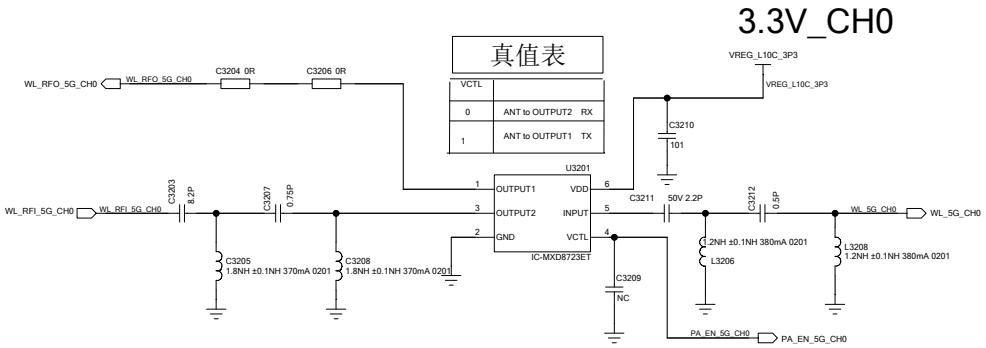
ANT6 2.4G CHAIN0 & 5G CHAIN0

1、测试座下方预留与0201封装相同大小铜皮，兼容去测试座方案；
2、EVT与DVT阶段上测试座，铜皮上绿油；
3、试产评估OK后，PVT阶段加上0R电阻，测试座NC

CH0 2.4G



CH0 5G

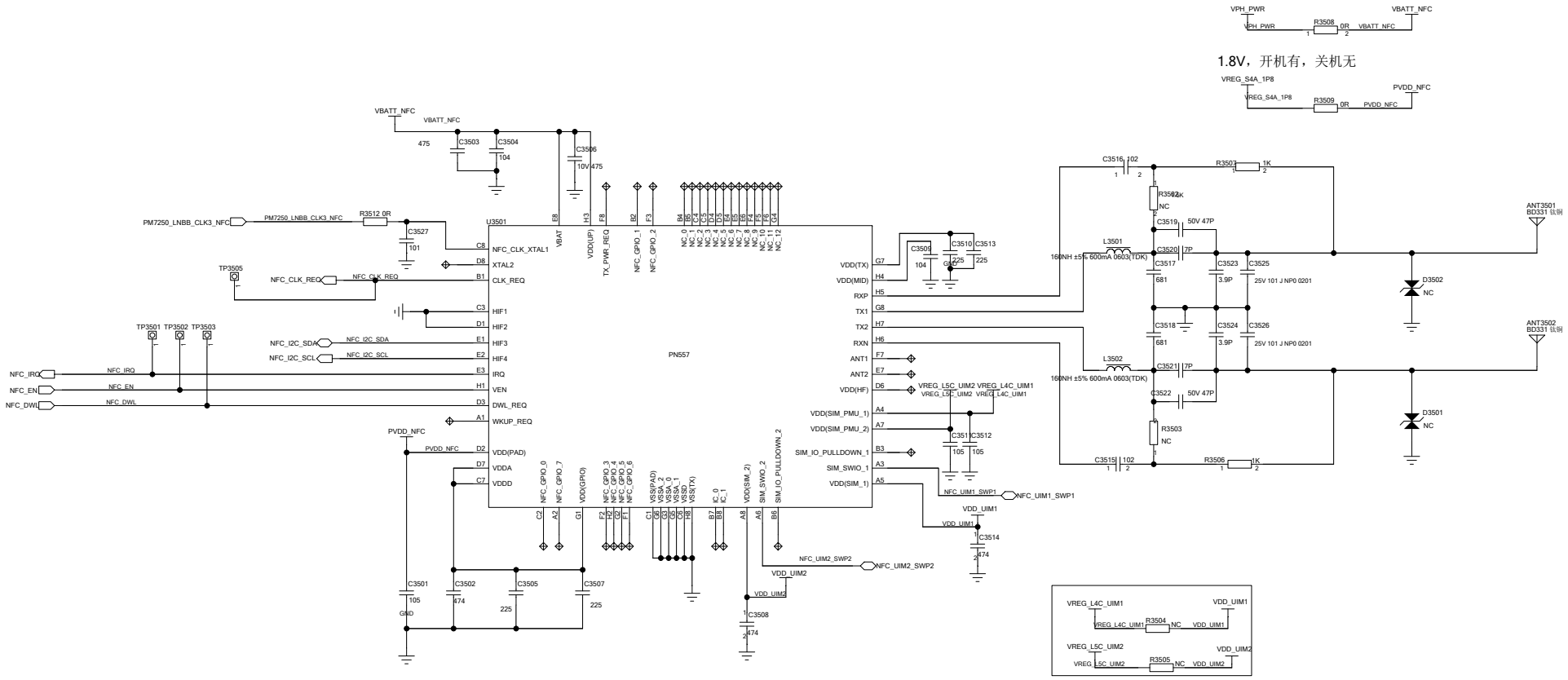


VCTL	
0	ANT to OUTPUT2 RX
1	ANT to OUTPUT1 TX

	Sign	Date	Type:	
Drawn By			Draw No:	
Checked By			Sheet 2 of	Ver:
Standard By			oppo	
Approved By				

Schematic

NFC



	Sign	Date	Type:
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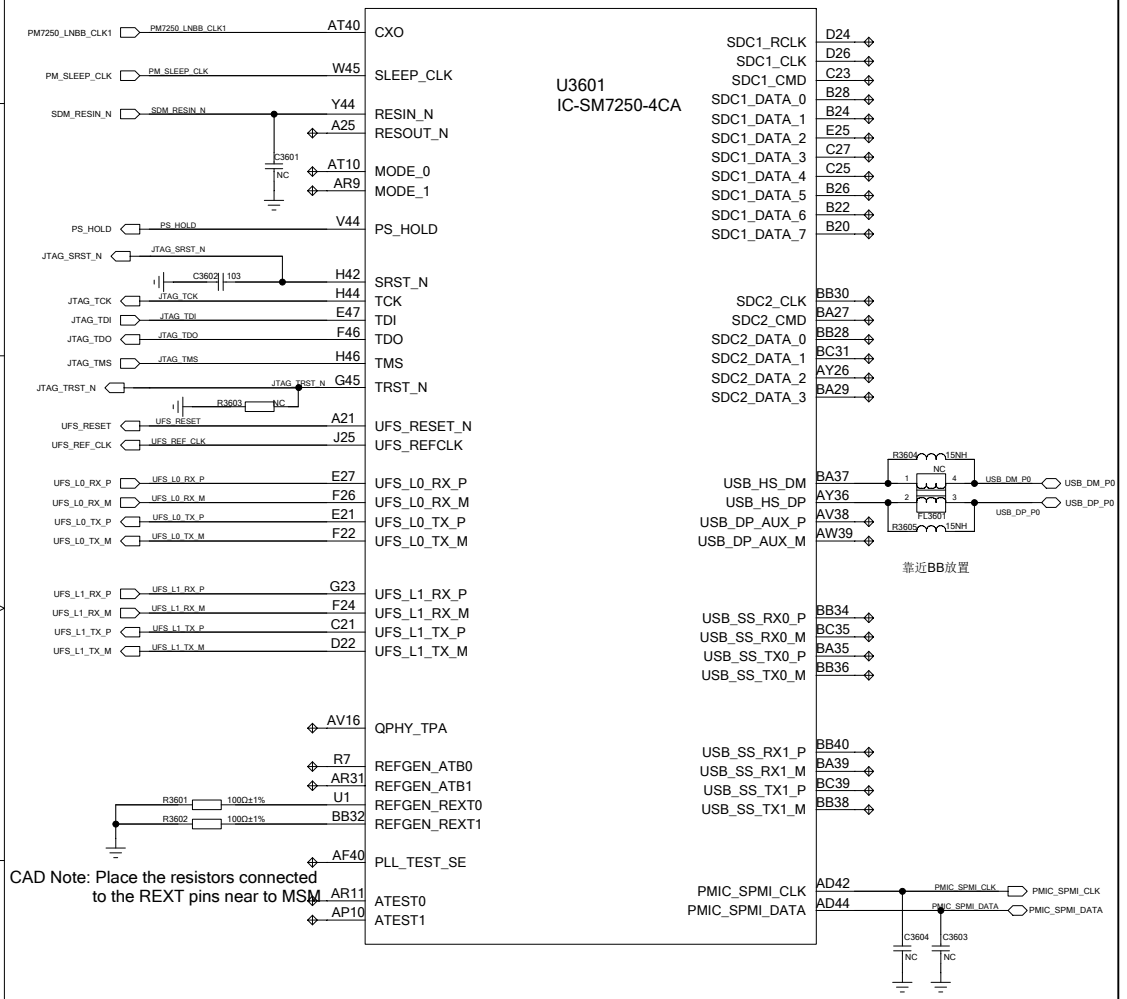
Checked By			Sheet of 21 Ver:
Standard By			oppo
Approved By			

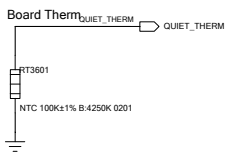
SM7250_SDC & USB



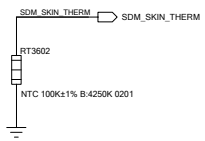
CAD Note: Place the resistors connected to the REXT pins near to MSM

CAD Note: Route the SPMI signals in Daisy Chain/Start routing from MSM to the PMICS to avoid stubs

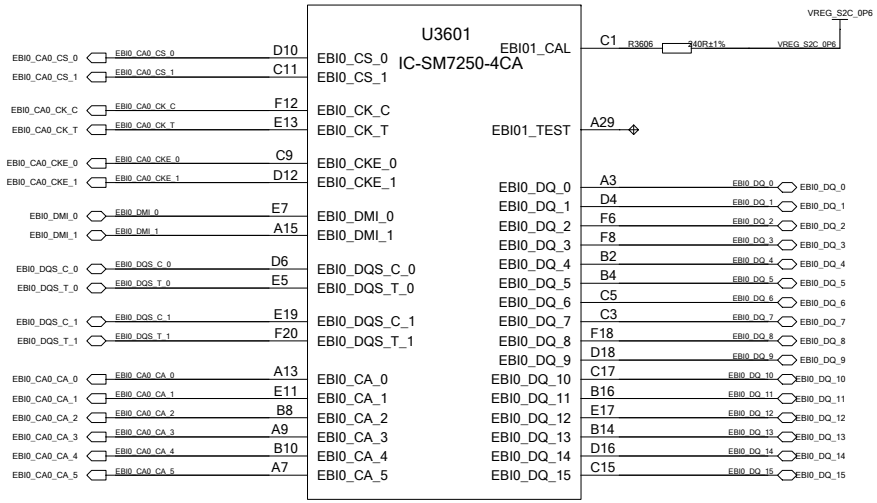
Board Therm

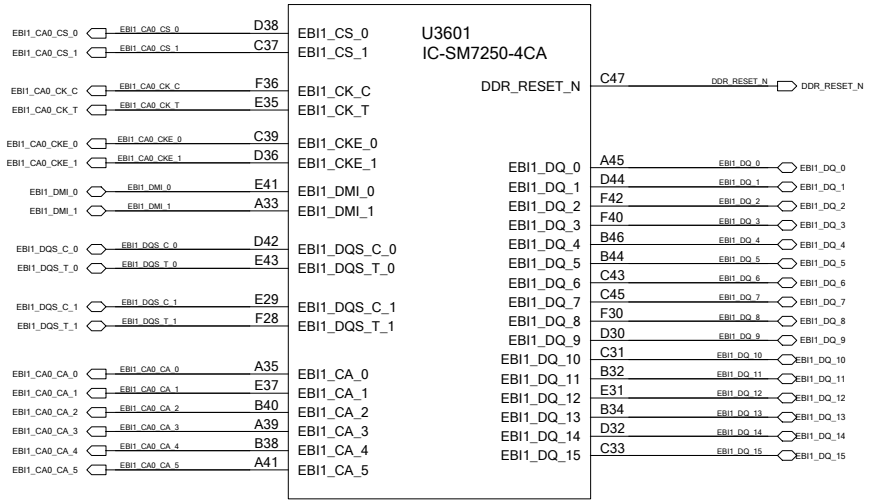


Place near SDM



SM7250_EBI0/1





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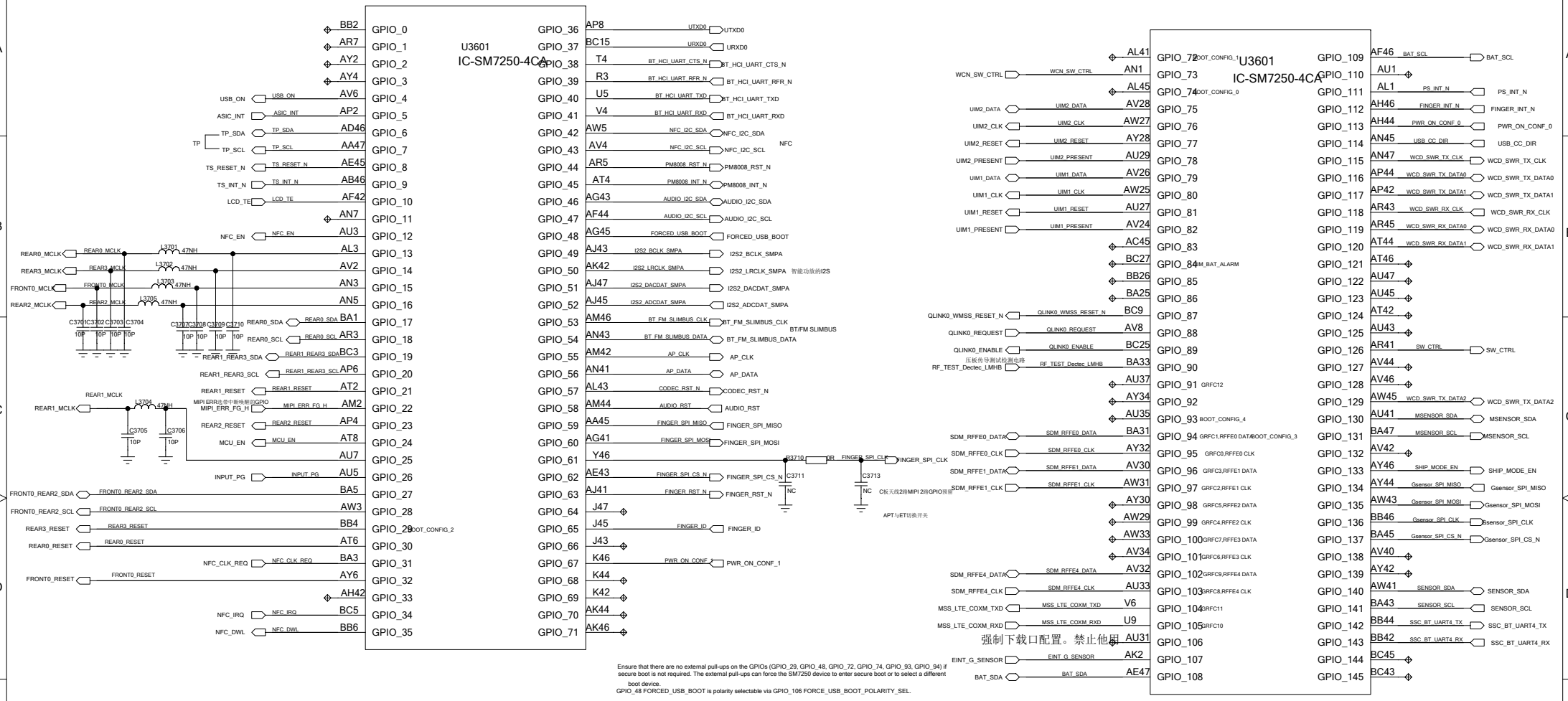
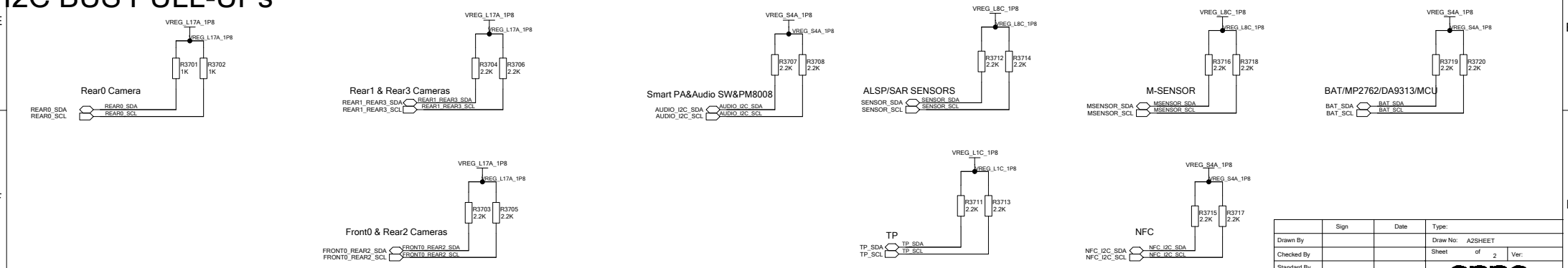
Drawn By			Draw No:
Checked By			Sheet of 53 Ver:
Standard By			oppo
Approved By			

SM7250_ GPIOs



I2C BUS PULL-UPs



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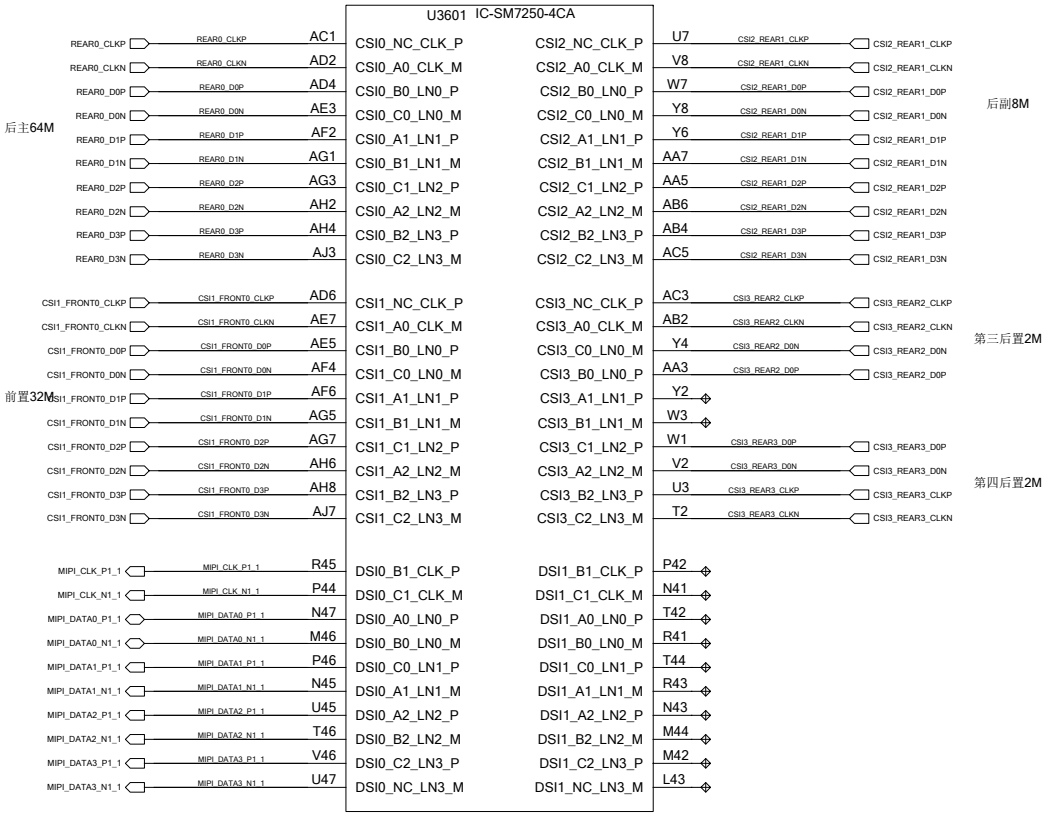
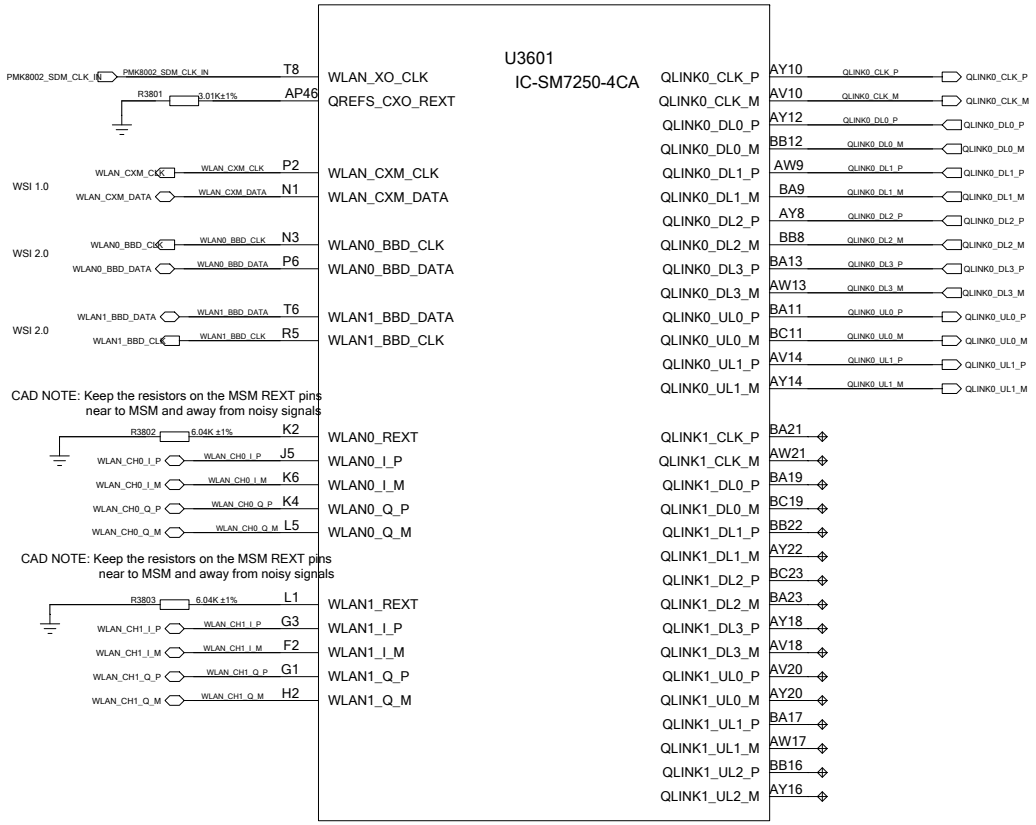
Checked By			Sheet of 2	Ver:
Standard By			oppo	
Approved By				

SDM7250_MIPI_ CSI&DSI

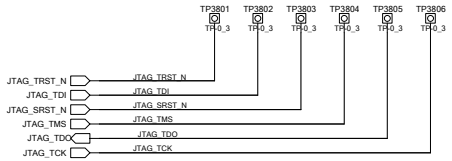


SDM7250_WCSS/RF



JTAG TEST POINT

布局在bottom面屏蔽盖外



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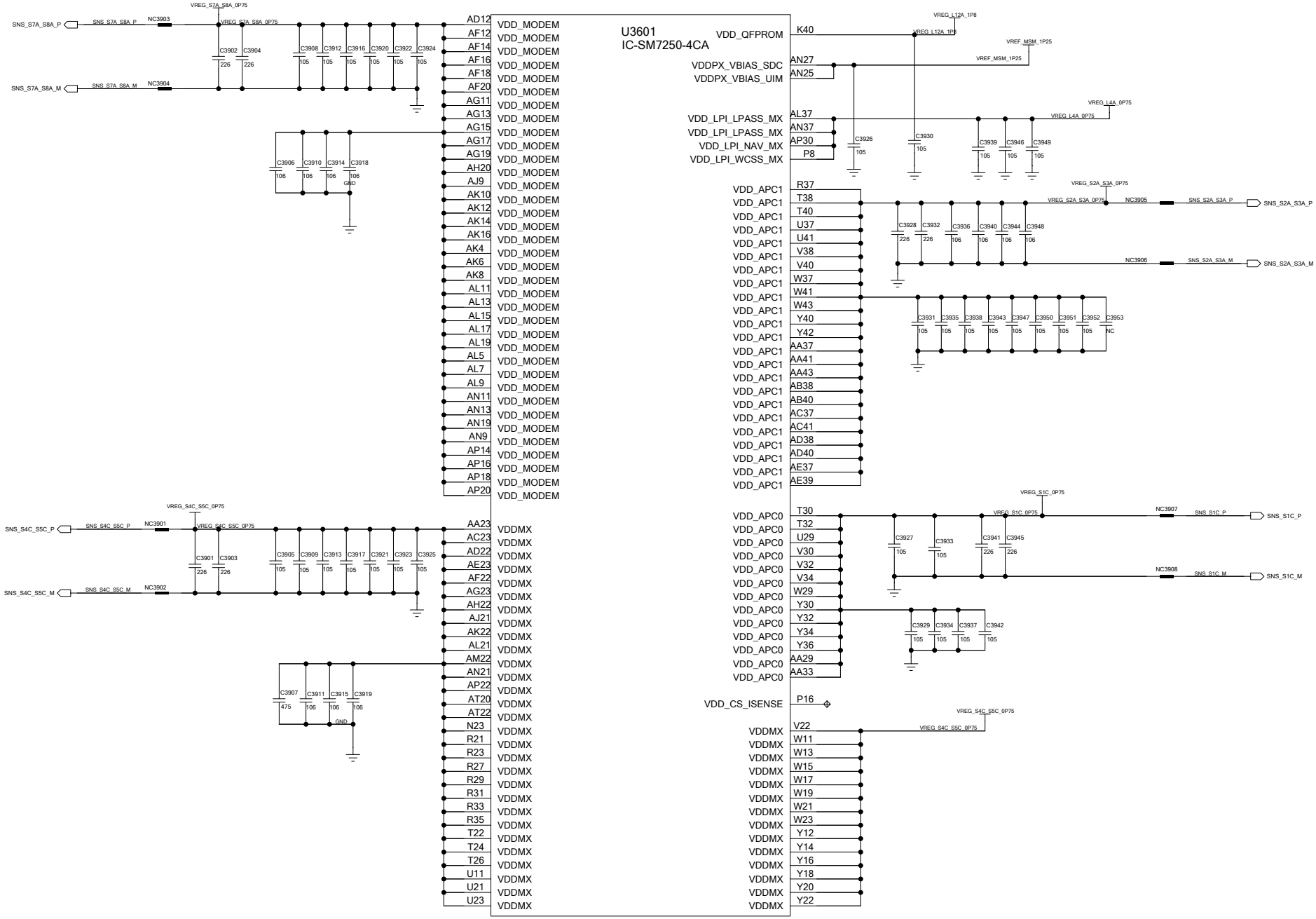

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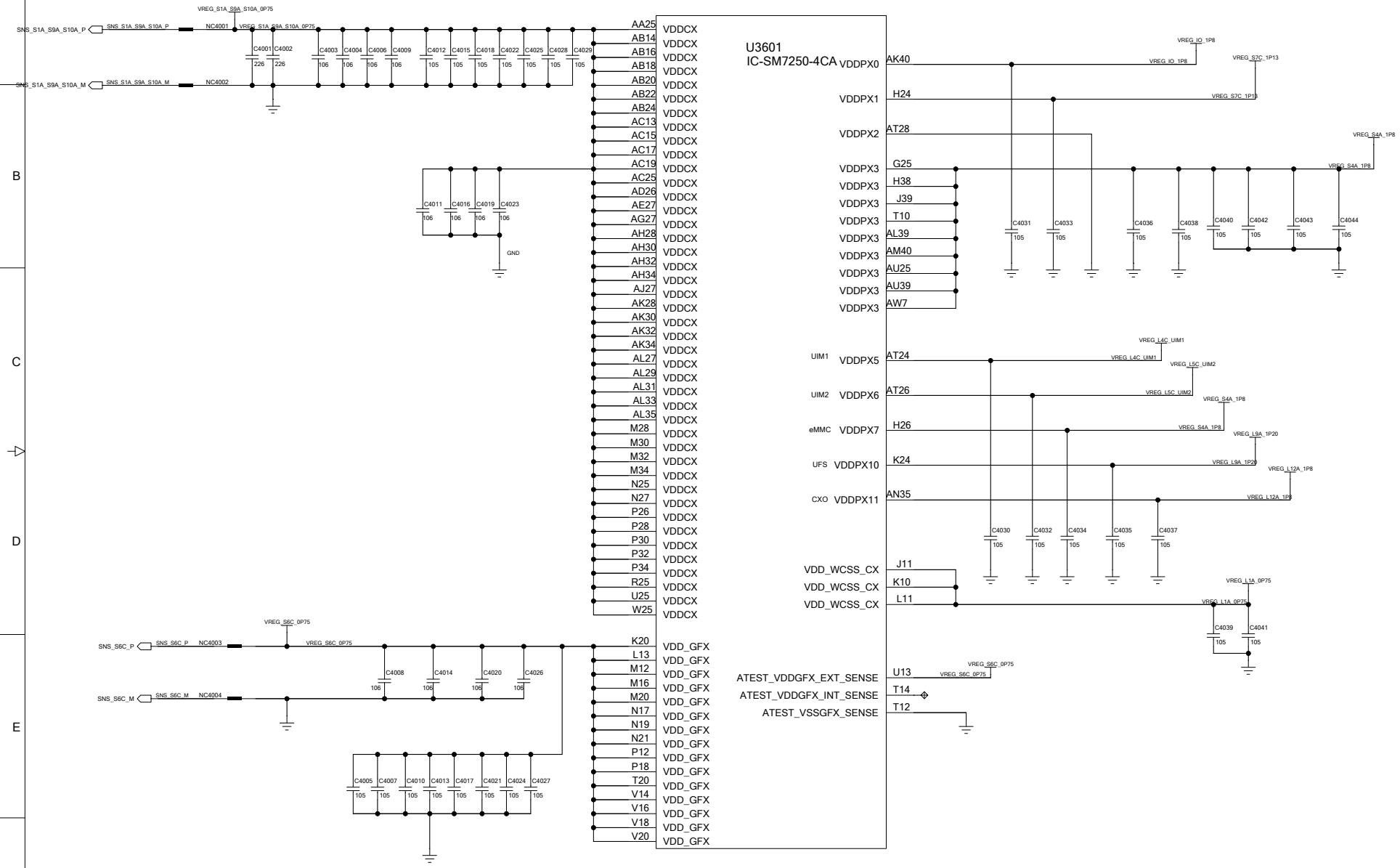
Approved By			



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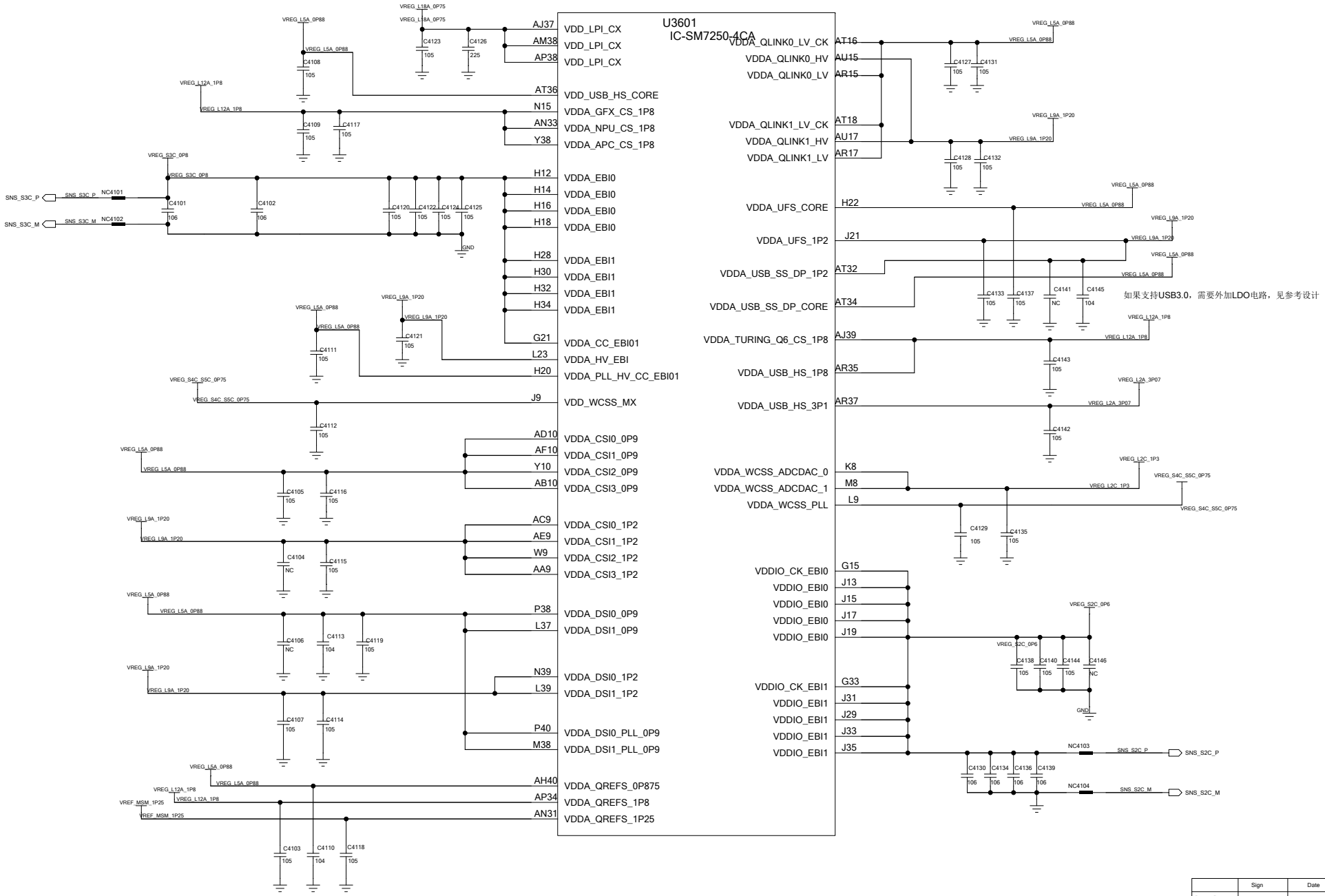

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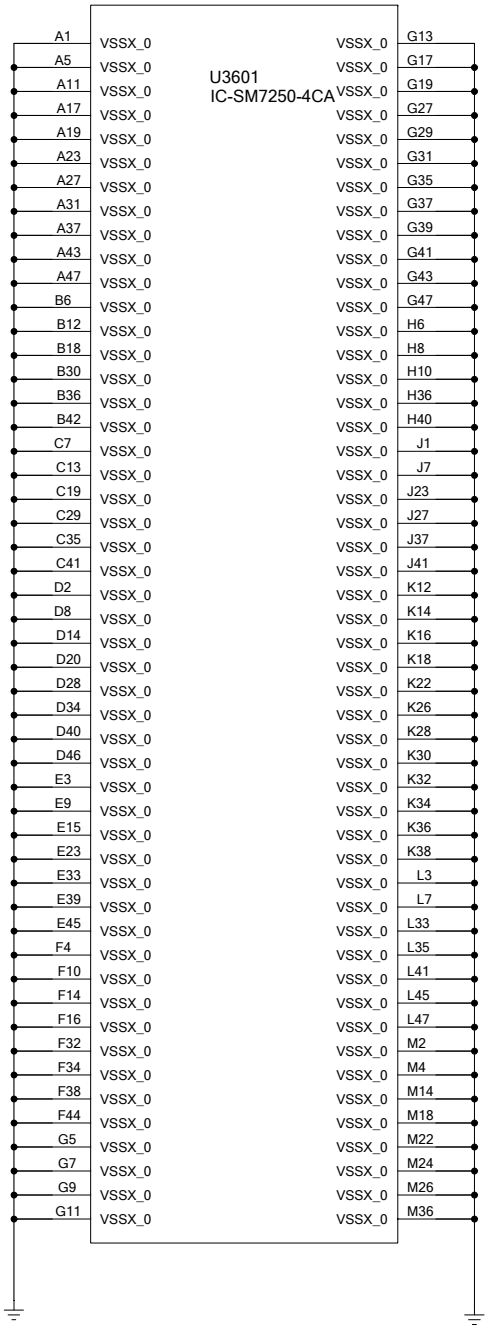
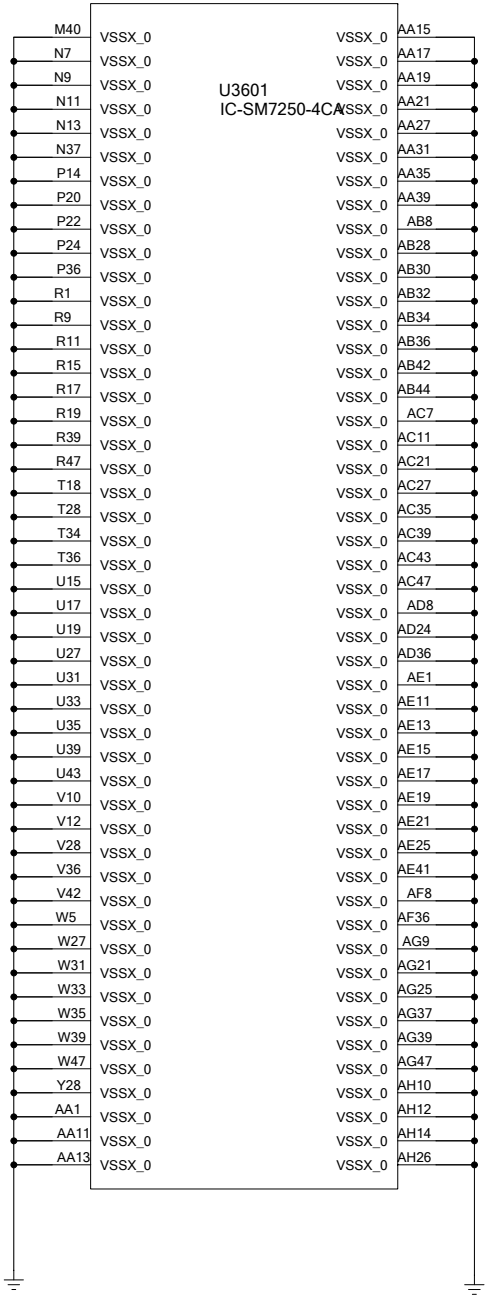
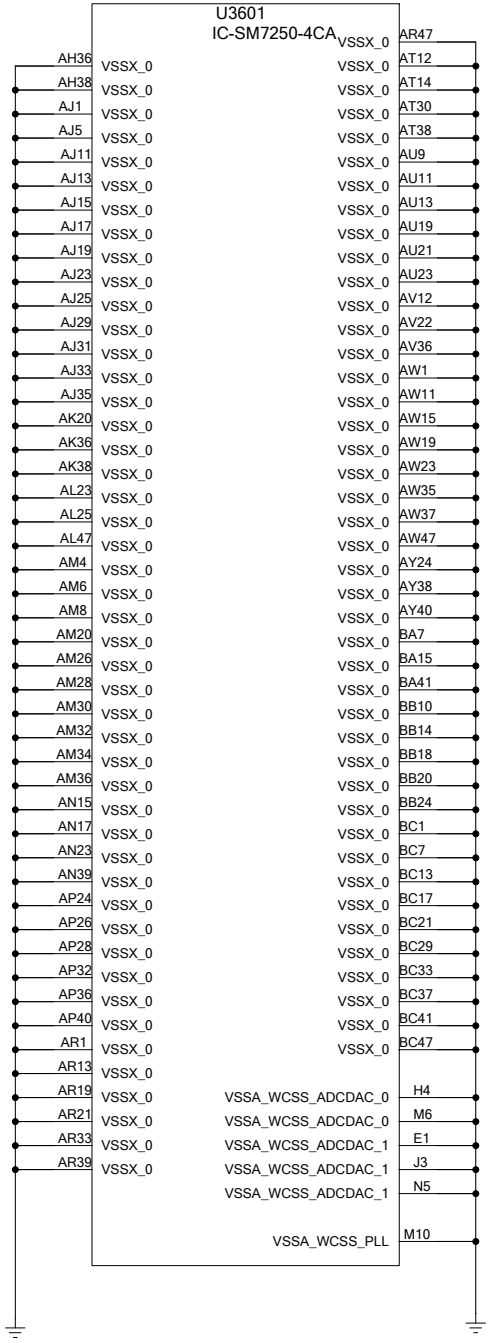
Standard By			oppo	
Approved By				







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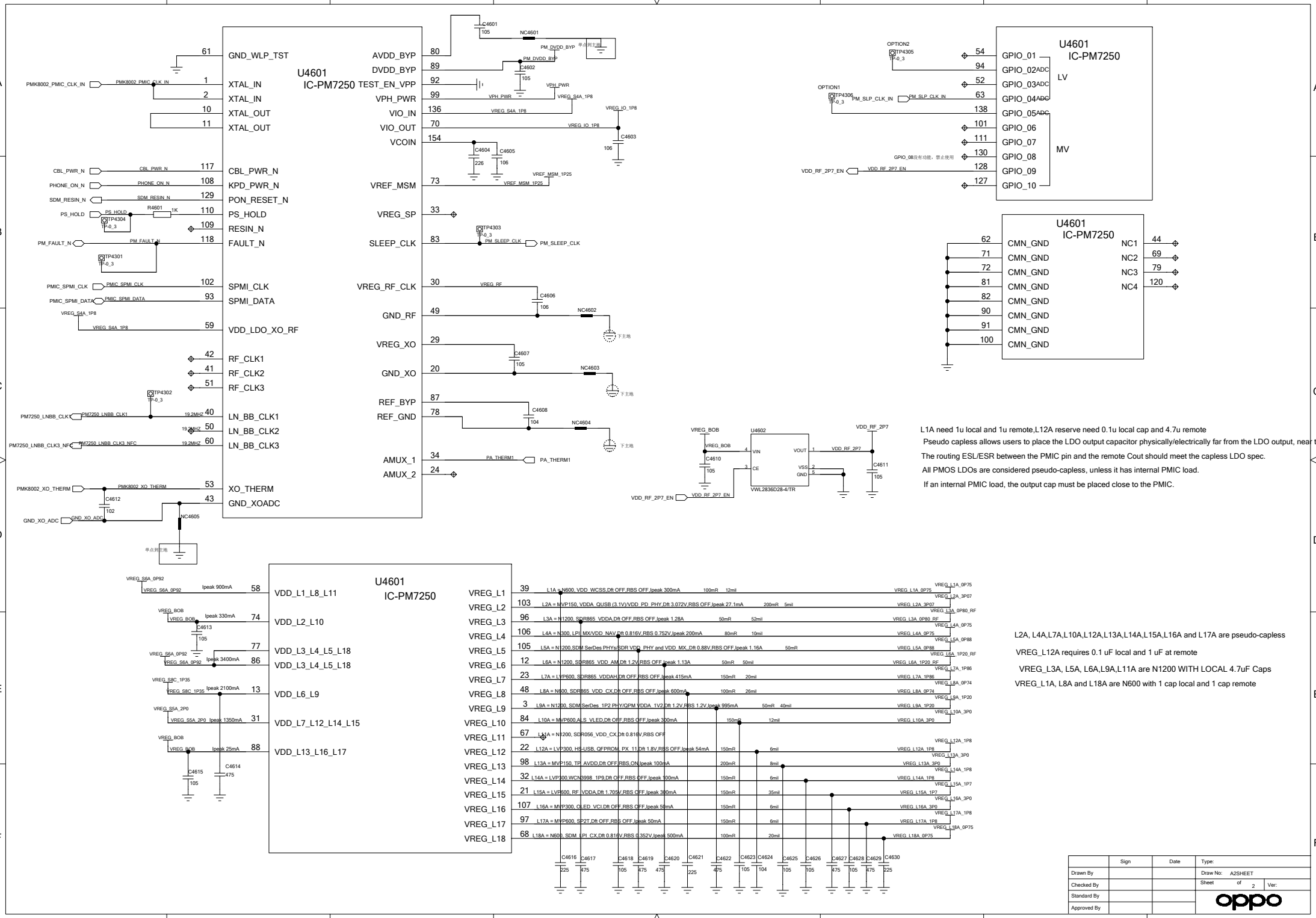
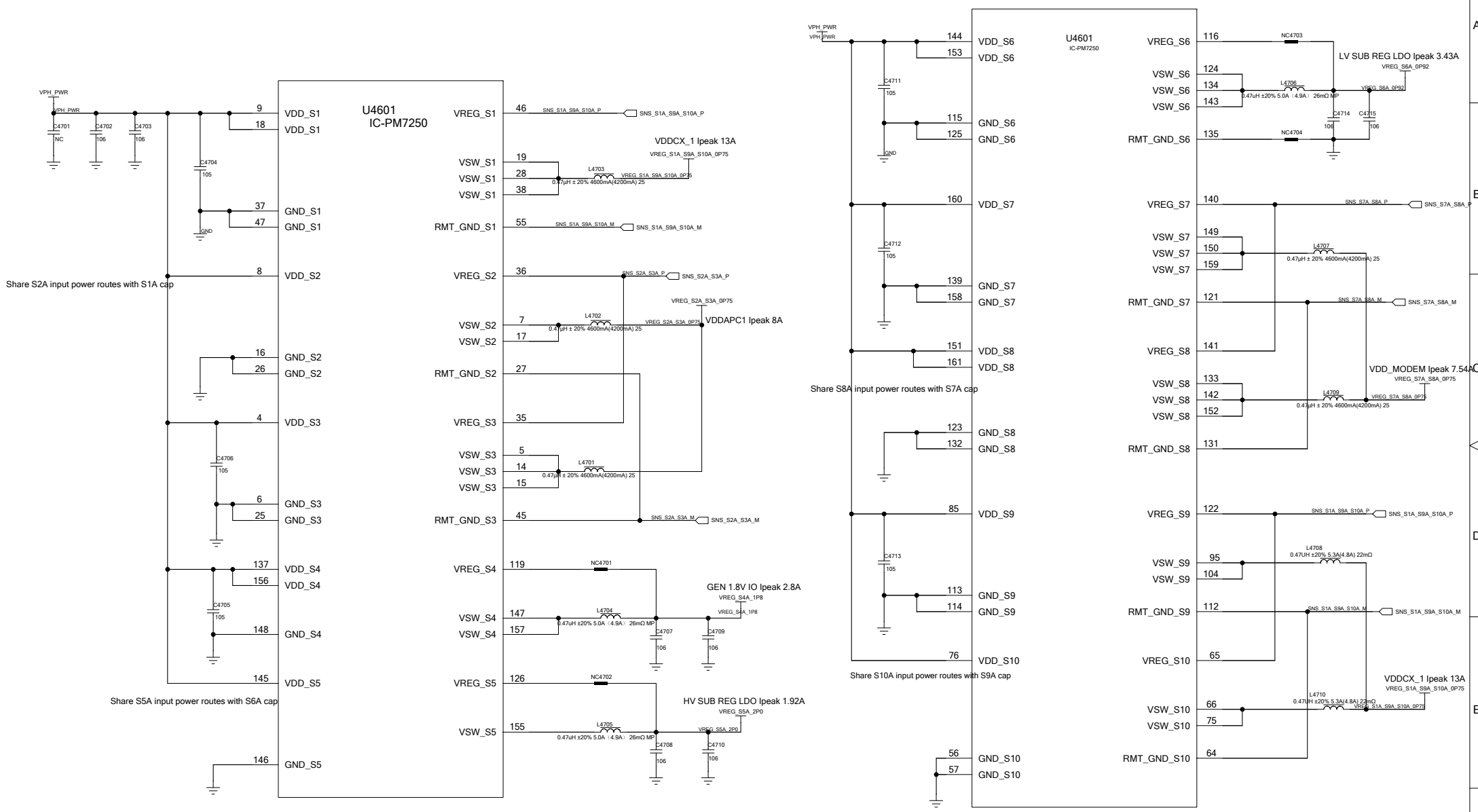
Approved By			

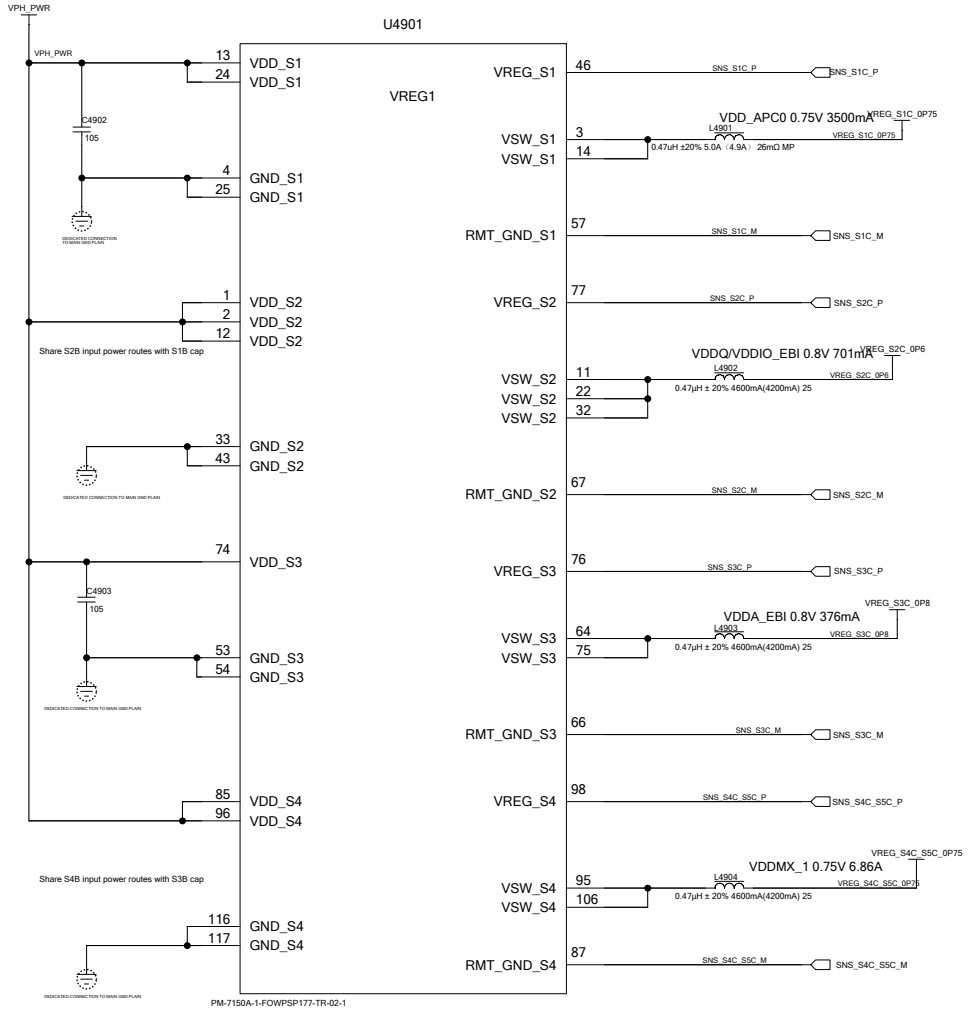

U4601
IC-PM7250
GND_WLP_TST
XTAL_IN
XTAL_IN
XTAL_OUT
XTAL_OUT
CBL_PWR_N
KPD_PWR_N
PON_RESET_N
PS_HOLD
RESIN_N
FAULT_N
SPMI_CLK
SPMI_DATA
VDD_LDO_XO_RF
RF_CLK1
RF_CLK2
RF_CLK3
LN_BB_CLK1
LN_BB_CLK2
LN_BB_CLK3
XO_THERM
GND_XOADC
AVDD_BYP
DVDD_BYP
TEST_EN_VPP
VPH_PWR
VIO_IN
VIO_OUT
VCOIN
VREF_MSM
VREG_SP
SLEEP_CLK
VREG_RF_CLK
GND_RF
VREG_XO
GND_XO
REF_BYP
REF_GND
AMUX_1
AMUX_2
PMK8002_PMIC_CLK_IN
PMK8002_XO_THERM
GND_XO_ADC
PM7250_LNBB_CLK1
PM7250_LNBB_CLK3_NFC
PA_THERM1
PM_SLEEP_CLK
PM_DVDD_BYP
VREG_S4A_1P8
VREG_IO_1P8
VREG_MSM_1P25
VREG_RF
NC4601
NC4602
NC4603
NC4604
NC4605
单点到主地
下主地
U4601
IC-PM7250
GPIO_01
GPIO_02ADC
GPIO_03ADC
GPIO_04ADC
GPIO_05ADC
GPIO_06
GPIO_07
GPIO_08
GPIO_09
GPIO_10
LV
MV
OPTION1
OPTION2
PM_SLP_CLK_IN
VDD_RF_2P7_EN
GPIO_08没有功能，禁止使用
U4601
IC-PM7250
CMN_GND
NC1
NC2
NC3
NC4
U4602
VWL2836D28-4/TR
VREG_BOB
VDD_RF_2P7
VDD_RF_2P7_EN
U4601
IC-PM7250
VDD_L1_L8_L11
VDD_L2_L10
VDD_L3_L4_L5_L18
VDD_L6_L9
VDD_L7_L12_L14_L15
VDD_L13_L16_L17
VREG_L1
VREG_L2
VREG_L3
VREG_L4
VREG_L5
VREG_L6
VREG_L7
VREG_L8
VREG_L9
VREG_L10
VREG_L11
VREG_L12
VREG_L13
VREG_L14
VREG_L15
VREG_L16
VREG_L17
VREG_L18
L1A = N600, VDD_WCSS,Dft OFF,RBS OFF,Ipeak 300mA
L2A = MVP150, VDDA_QUSB (3.1V)/VDD_PD_PHY,Dft 3.072V,RBS OFF,Ipeak 27.1mA
L3A = N1200, SDR865_VDDA,Dft OFF,RBS OFF,Ipeak 1.28A
L4A = N300, LPI_MX/VDD_NAV,Dft 0.816V,RBS 0.752V,Ipeak 200mA
L5A = N1200,SDM SerDes PHYs/SDR VDD_PHY and VDD_MX,,Dft 0.88V,RBS OFF,Ipeak 1.16A
L6A = N1200, SDR865_VDD_AM,Dft 1.2V,RBS OFF,Ipeak 1.13A
L7A = LVP600, SDR865_VDDAH,Dft OFF,RBS OFF,Ipeak 415mA
L8A = N600, SDR865_VDD_CX,Dft OFF,RBS OFF,Ipeak 600mA
L9A = N1200, SDM SerDes_1P2 PHY/QPM VDDA_1V2,Dft 1.2V,RBS 1.2V,Ipeak 995mA
L10A = MVP600,ALS_VLED,Dft OFF,RBS OFF,Ipeak 300mA
L11A = N1200, SDR056_VDD_CX,Dft 0.816V,RBS OFF
L12A = LVP300, HS-USB, QFPROM, PX_11,Dft 1.8V,RBS OFF,Ipeak 54mA
L13A = MVP150, TP_AVDD,Dft OFF,RBS,ON,Ipeak 100mA
L14A = LVP300,WCN3998_1P9,Dft OFF,RBS OFF,Ipeak 100mA
L15A = LVP600, RF_VDDA,Dft 1.705V,RBS OFF,Ipeak 300mA
L16A = MVP300, OLED_VCI,Dft OFF,RBS OFF,Ipeak 50mA
L17A = MVP600, SP2T,Dft OFF,RBS OFF,Ipeak 50mA
L18A = N600, SDM_LPI_CX,Dft 0.816V,RBS 0.352V,Ipeak 500mA
L1A need 1u local and 1u remote,L12A reserve need 0.1u local cap and 4.7u remote
Pseudo capless allows users to place the LDO output capacitor physically/electrically far from the LDO output, near the lo
The routing ESL/ESR between the PMIC pin and the remote Cout should meet the capless LDO spec.
All PMOS LDOs are considered pseudo-capless, unless it has internal PMIC load.
If an internal PMIC load, the output cap must be placed close to the PMIC.
L2A, L4A,L7A,L10A,L12A,L13A,L14A,L15A,L16A and L17A are pseudo-capless
VREG_L12A requires 0.1 uF local and 1 uF at remote
VREG_L3A, L5A, L6A,L9A,L11A are N1200 WITH LOCAL 4.7uF Caps
VREG_L1A, L8A and L18A are N600 with 1 cap local and 1 cap remote
Sign
Date
Type:
Drawn By
Draw No: A2SHEET
Checked By
Sheet of 2
Ver:
Standard By
Approved By
oppo

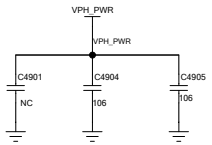


Do the simulation of the "cross impedance" for buck inputs
Star-routing for the shared input caps

	Sign	Date	Type: 38_PM7250_DCDC
Drawn By			Draw No:
Checked By			Sheet of 53 Ver:
Standard By			oppo
Approved By			

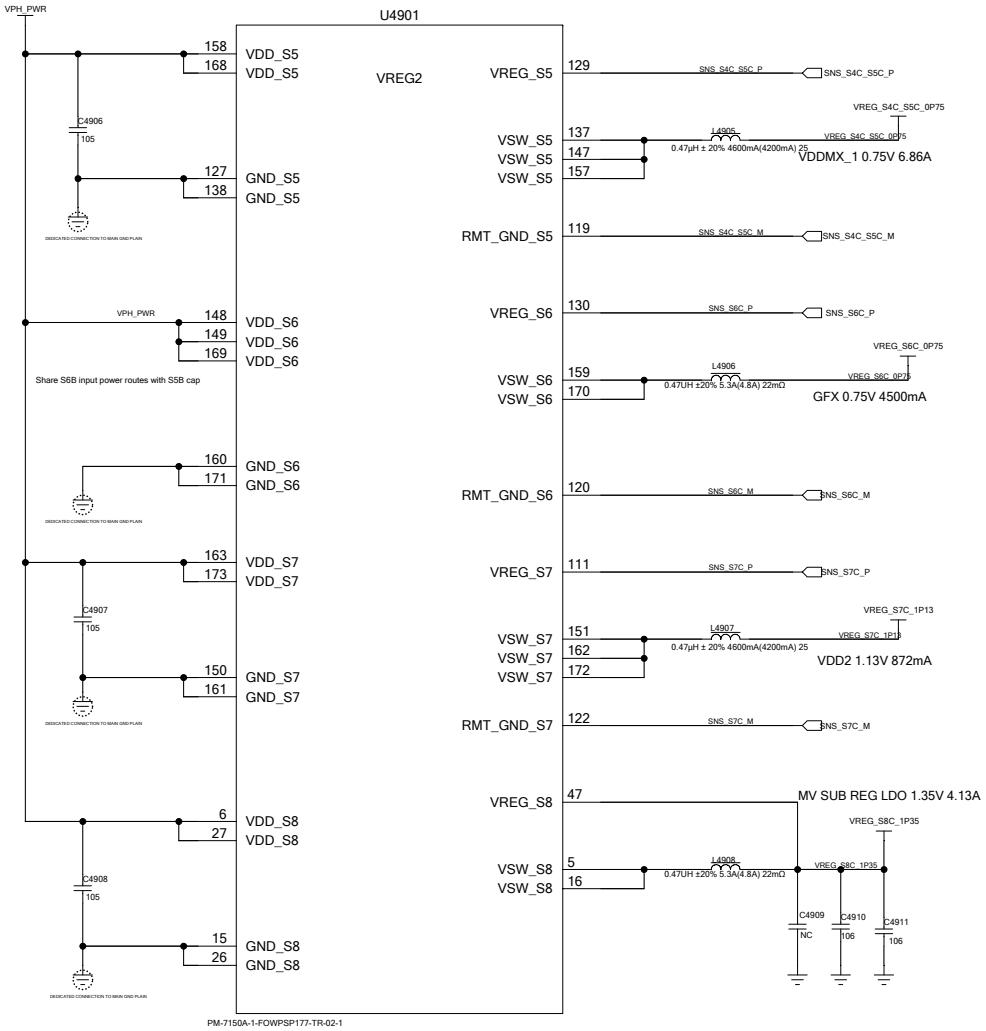
PM7150A_SMPS_1





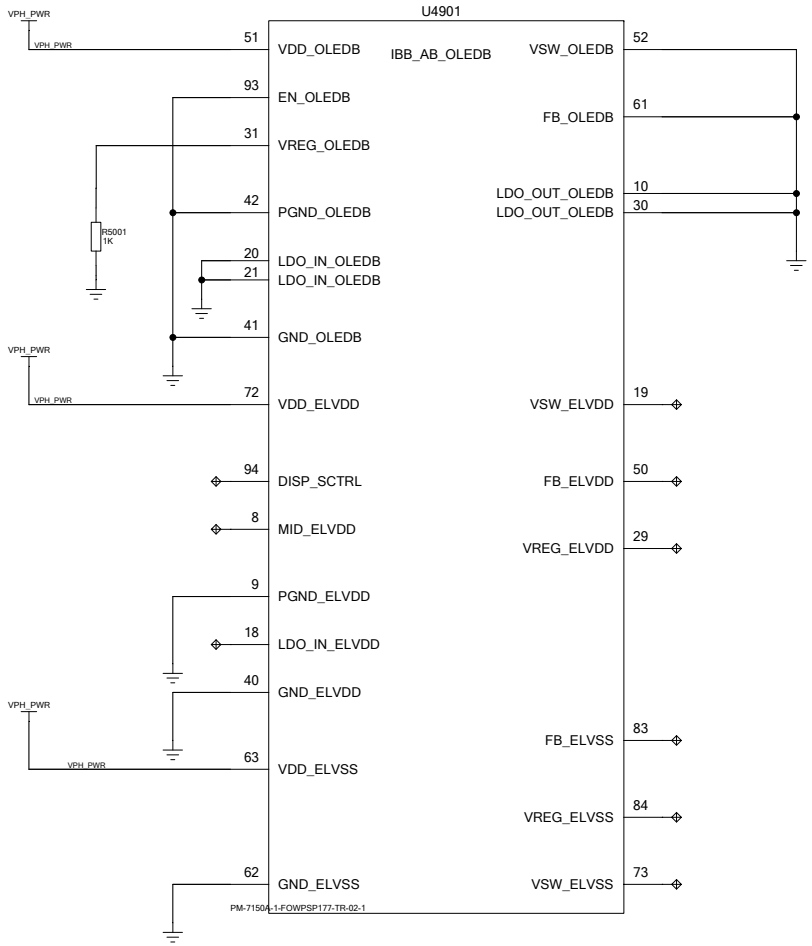
Make sure these bulk caps are distributed across PM7150A. Don't place these caps in one place.

PM7150A_SMPS_2

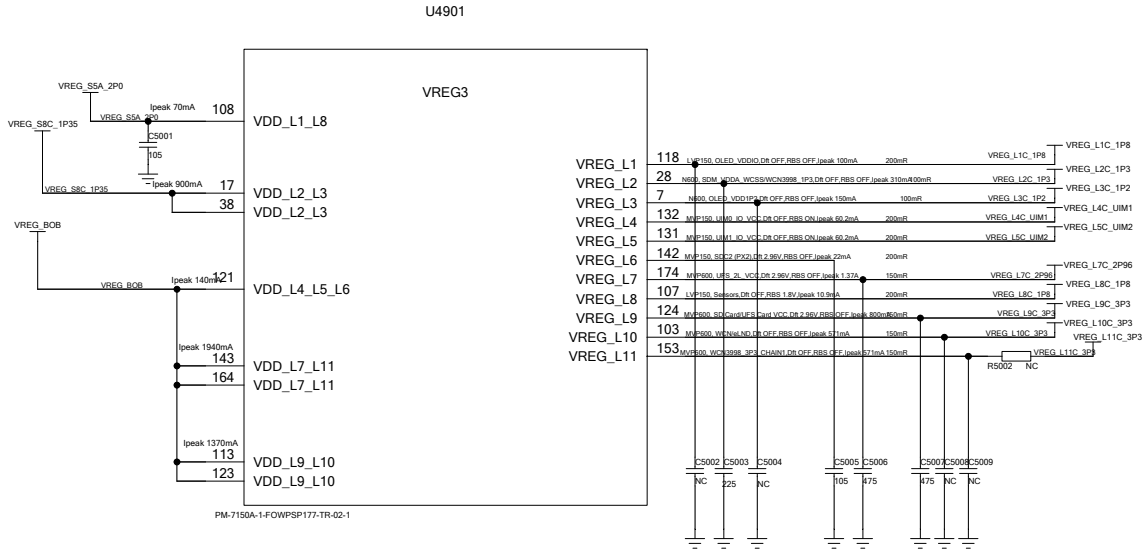


	Sign	Date	Type: 39_PM7150A-DCDC	
Drawn By			Draw No:	
Checked By			Sheet of 53	Ver:
Standard By			oppo	
Approved By				

PM7150A_OLED

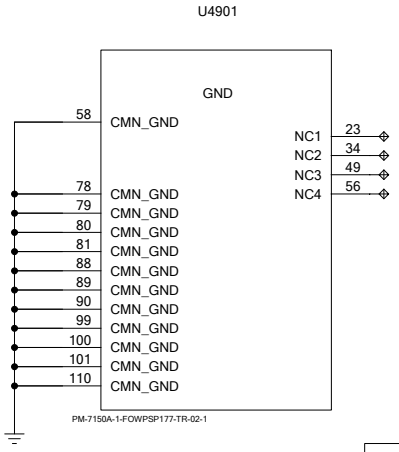


PM7150A_LDO



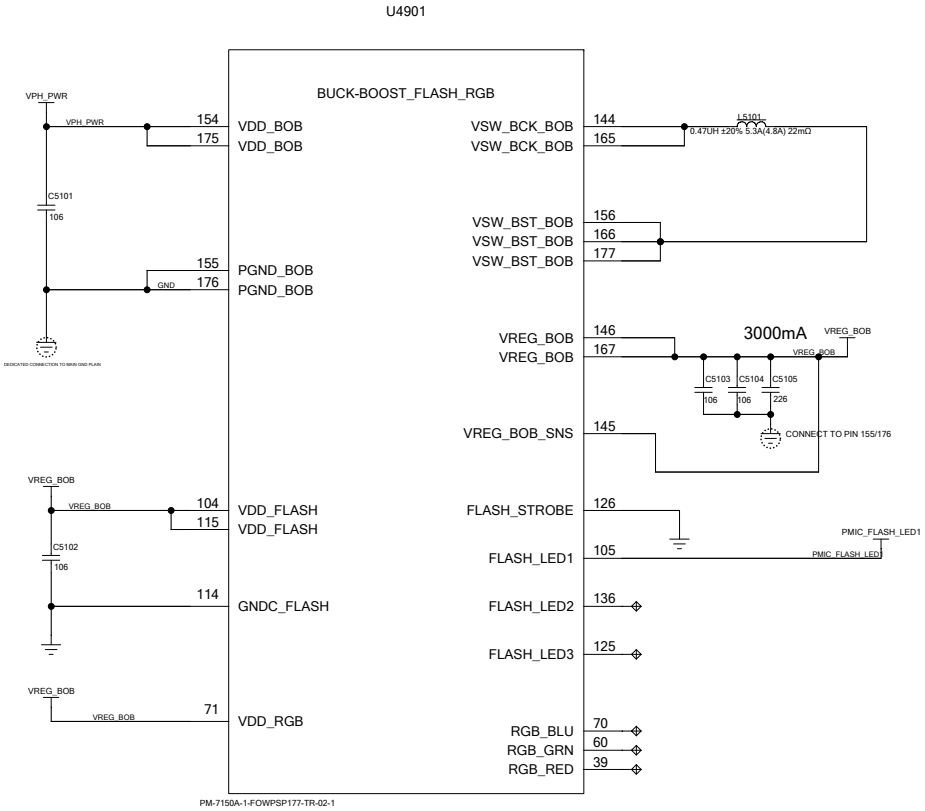
L1C, L4C,L5C,L6C,L7C,L8C,L9C,L10C and L11C are pseudo-capless
VREG_L2C and L3C are N600 with 1 cap local and 1 cap remote

PM7150A_GND



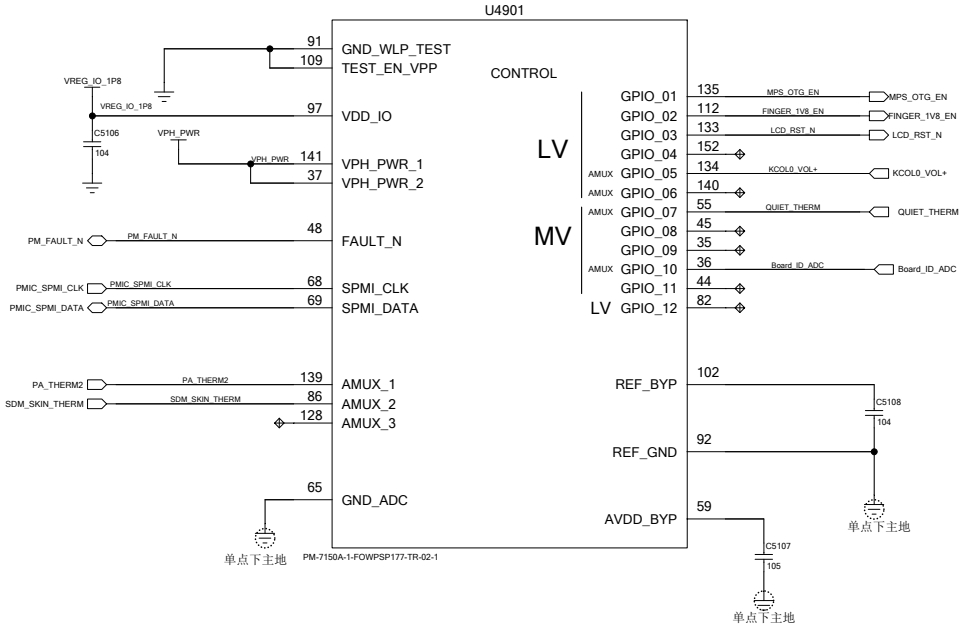
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet: 26 of 30 Ver:
Standard By			oppo
Approved By			

PM7150A_BOB_FLASH_LPG



Power source	Default	GPIO availability
VDD_MSM_IO(VREG_L13A_1p8)	1.8V	GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_8, GPIO_9, GPIO_11, GPIO_12 (LV)
VPH_PWR	3.6V	GPIO_1, GPIO_6, GPIO_7, GPIO_10 (MV)

PM7150A_GPIO

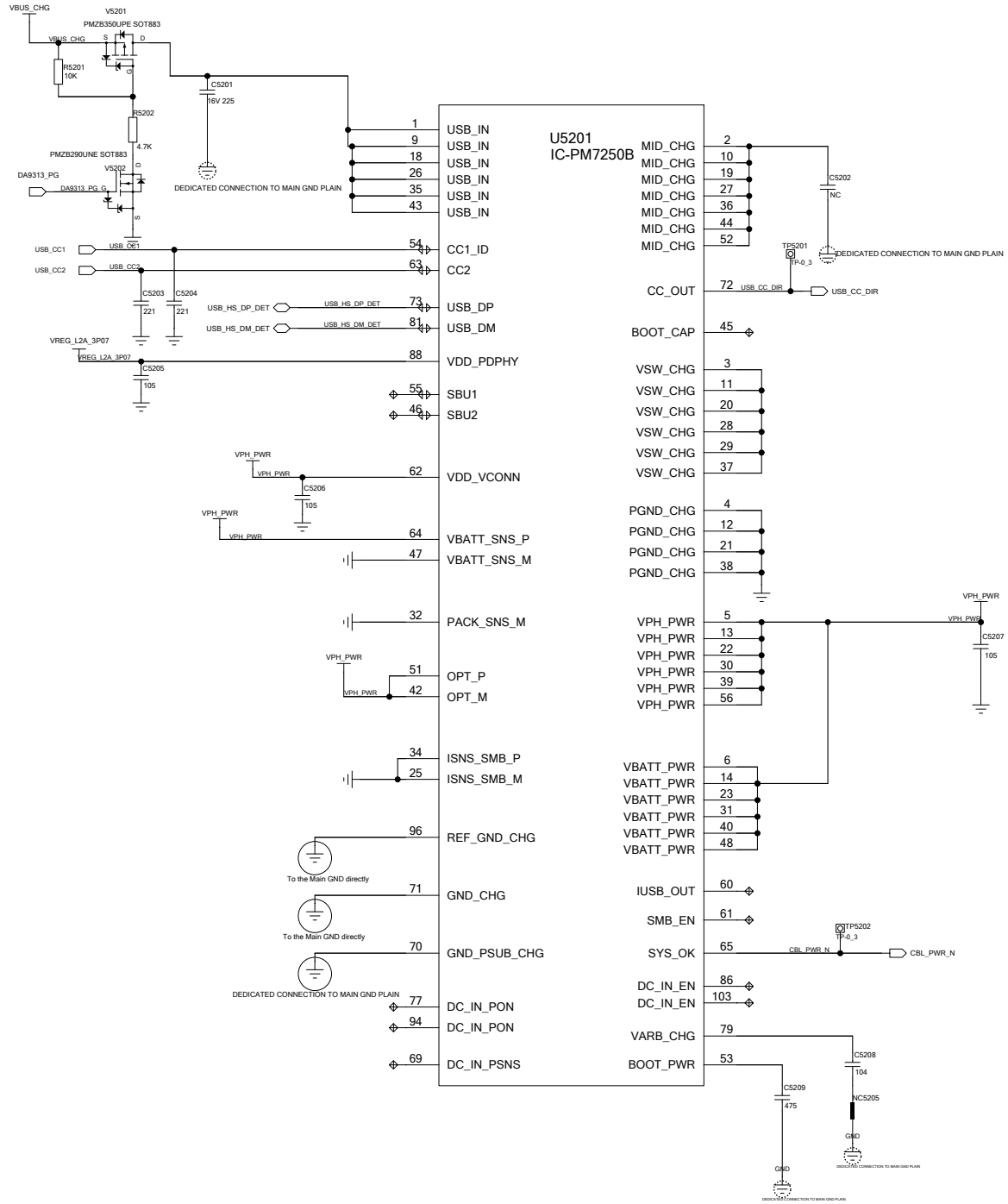


	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet: 27 of 32 Ver:
Standard By			
Approved By			

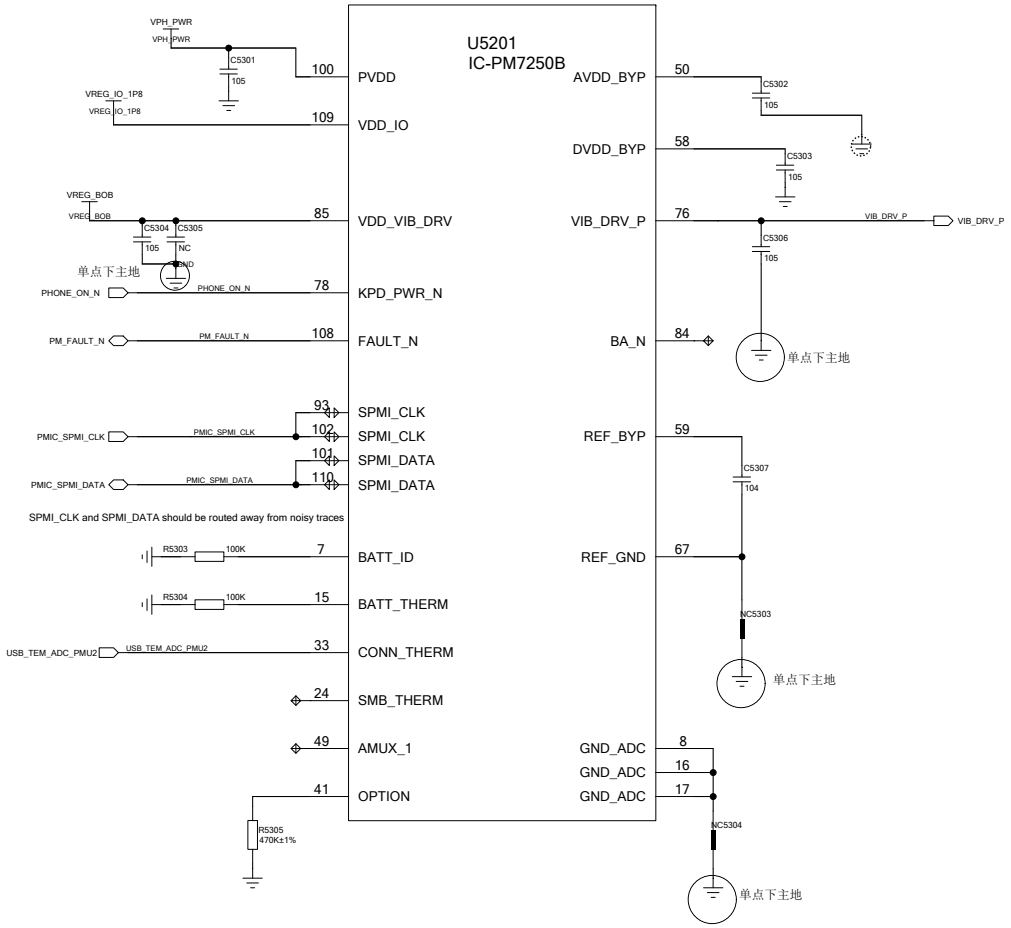
oppo

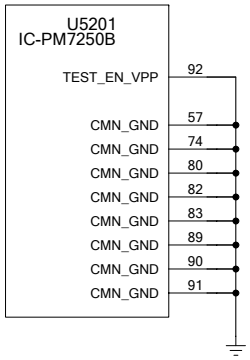
PM7250B_CHARGE/FG

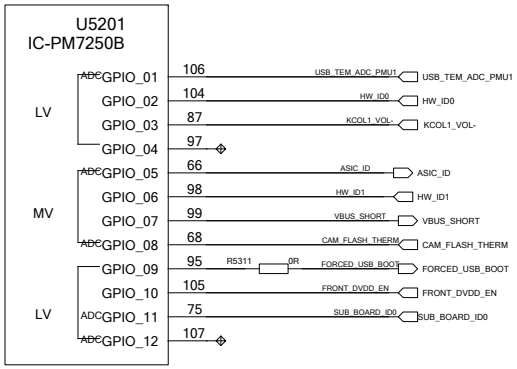
USB触发开机的延时电路



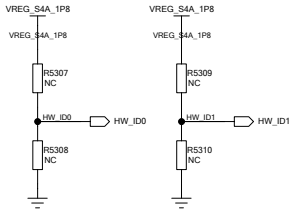
	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet of 30	Ver:
Standard By			oppo	
Approved By				

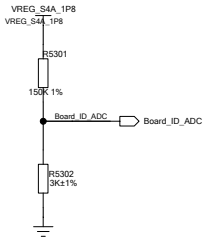


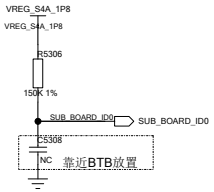




1. 开机时软件先设置输入pullup，读取IO状态0；再设置输入pulldown，读取IO状态1；最后设置为输入nopull
2. 上下拉电阻10K以内，不同平台需要确认所选GPIO上下拉电阻阻值，确保外部上下拉能拉高/低

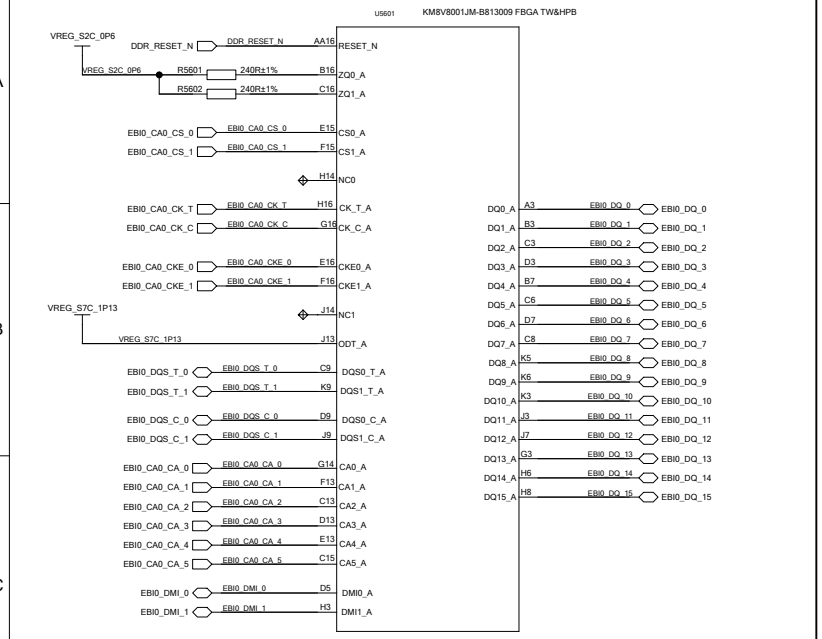




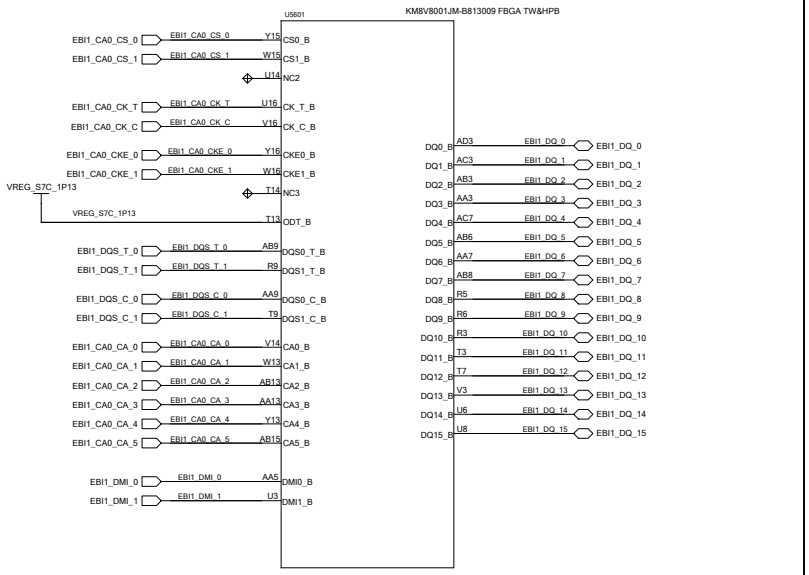


	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet of 30	Ver:
Standard By			oppo	
Approved By				

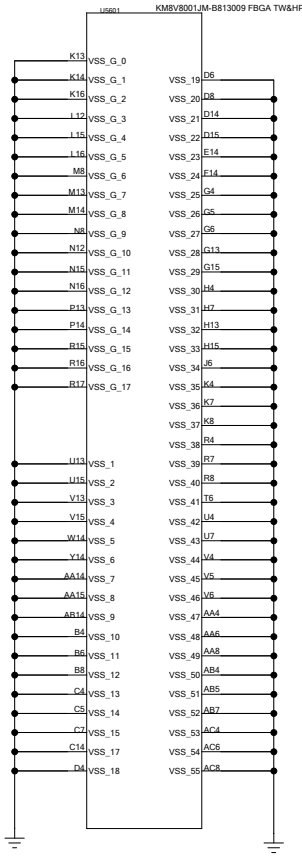
uMCP_EBI0



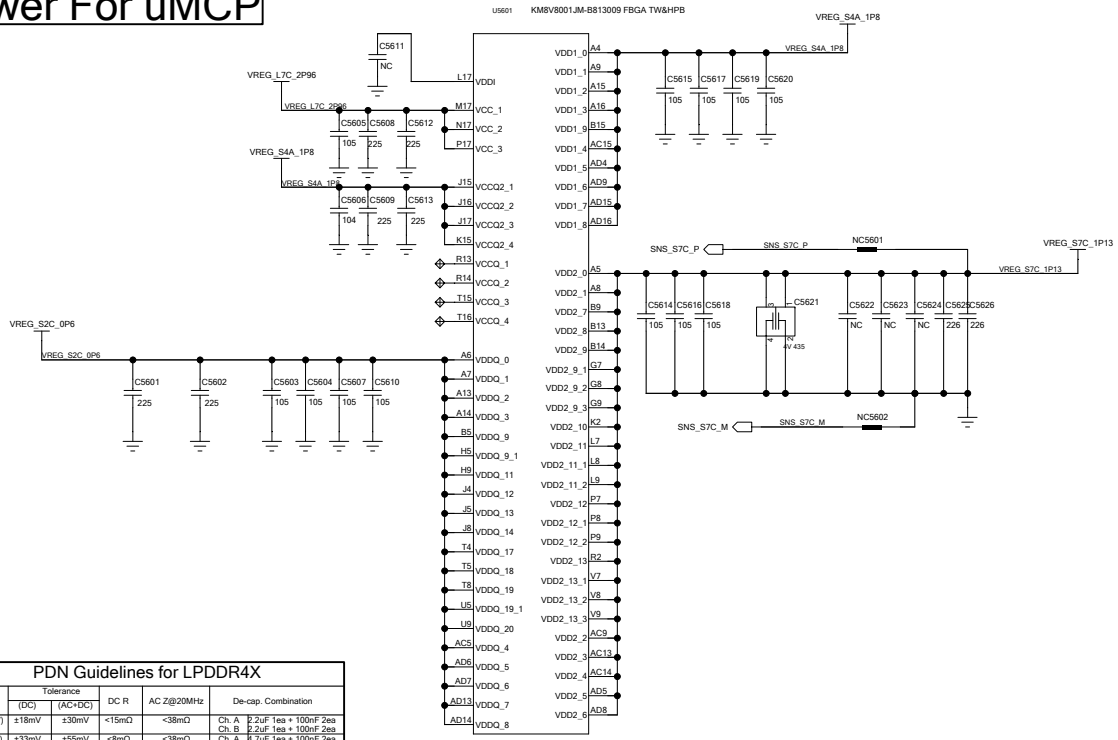
uMCP_EBI1



uMCP_GND

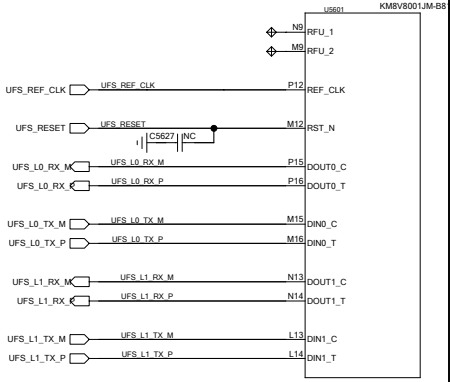


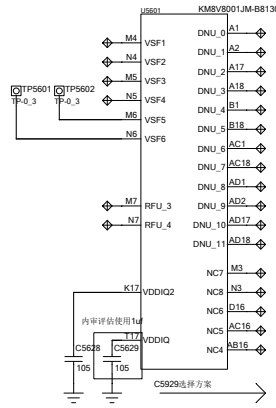
Power For uMCP



PDN Guidelines for LPDDR4X						
	Tolerance		DC R	AC Z@20MHz	De-cap. Combination	
	(DC)	(AC+DC)				
VDDQ(0.6V)	±18mV	±30mV	<15mΩ	<38mΩ	Ch. A Ch. B	2.2uF 1ea + 100nF 2ea 2.2uF 1ea + 100nF 2ea
VDD2(1.1V)	±33mV	±55mV	<8mΩ	<38mΩ	Ch. A Ch. B	4.7uF 1ea + 100nF 2ea 4.7uF 1ea + 100nF 2ea
VDD1(1.8V)	±55mV	±90mV	<40mΩ	<126mΩ		(2.2uF + 100nF) * 2

uMCP_UFS



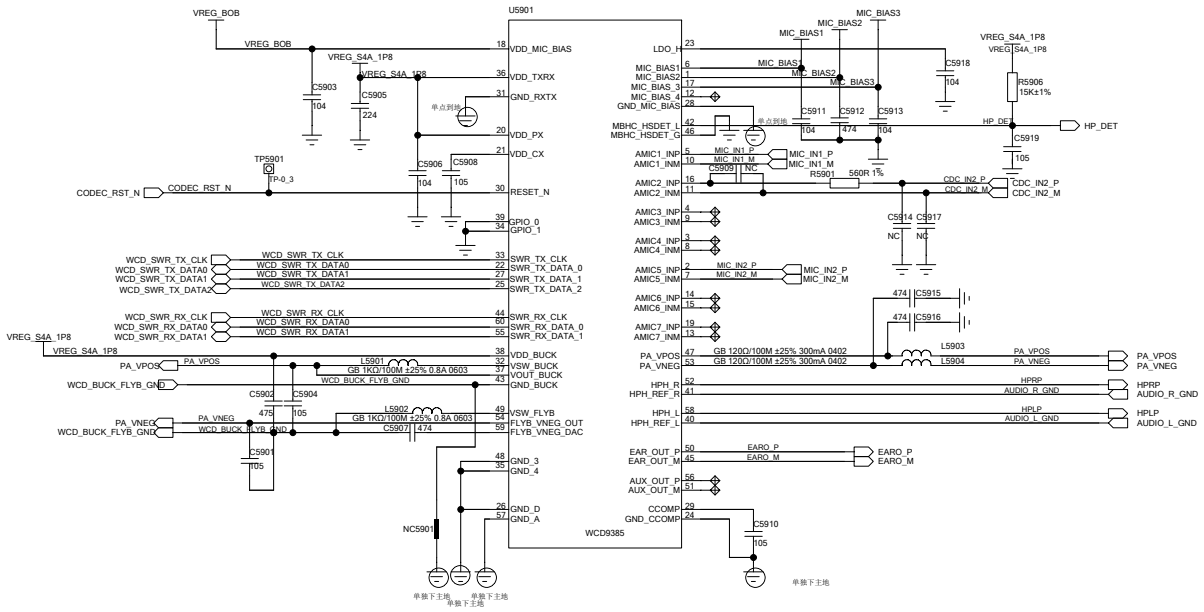


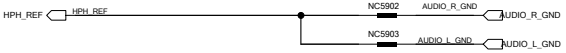
samsung	hynix	Micron	C5629
1	0	0	NC
1	1	0	0.22uF
1	1	1	1uF

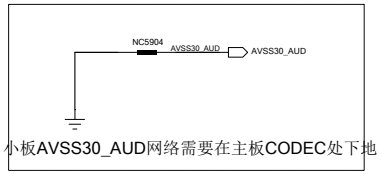
1代表使用
0代表不使用

	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet 12 of 32 Ver:
Standard By			oppo
Approved By			

WCD9385







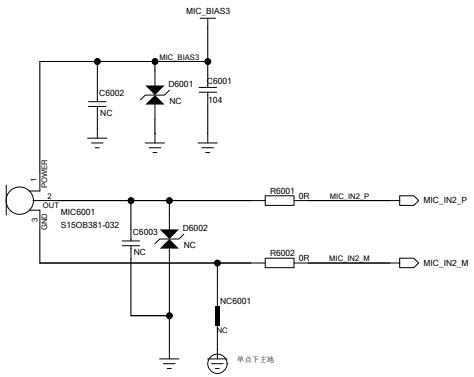
小板AVSS30_AUD网络需要在主板CODEC处下地

Power source	Default	GPIO availability
VDD_MSM_IO(VREG_L13A_1p8)	1.8V	GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_8, GPIO_9, GPIO_11, GPIO_12 (LV)
VPH_PWR	3.6V	GPIO_1, GPIO_6, GPIO_7, GPIO_10 (MV)

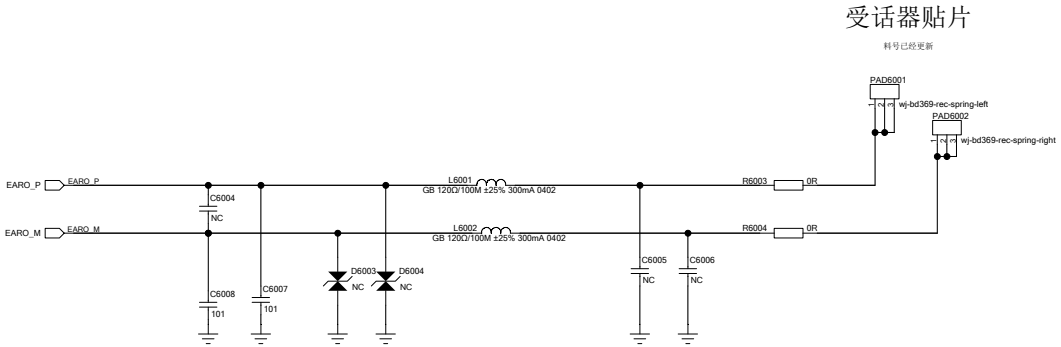
	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 32 of 32 Ver:
Standard By			
Approved By			

oppo

SUB MIC



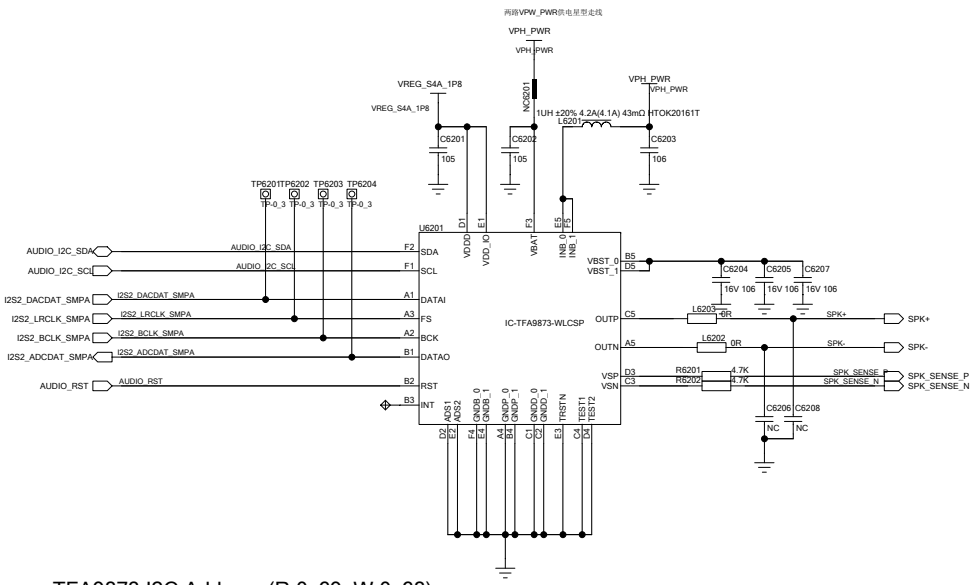
RECEIVER



	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet 32 of 32	Ver:
Standard By				
Approved By				

oppo

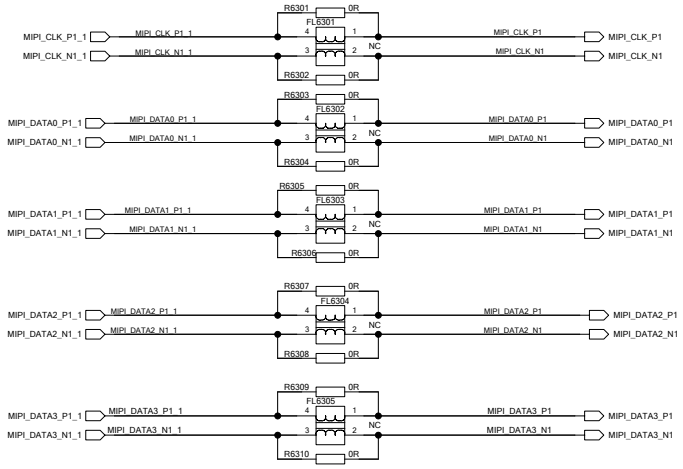
AUDIO PA



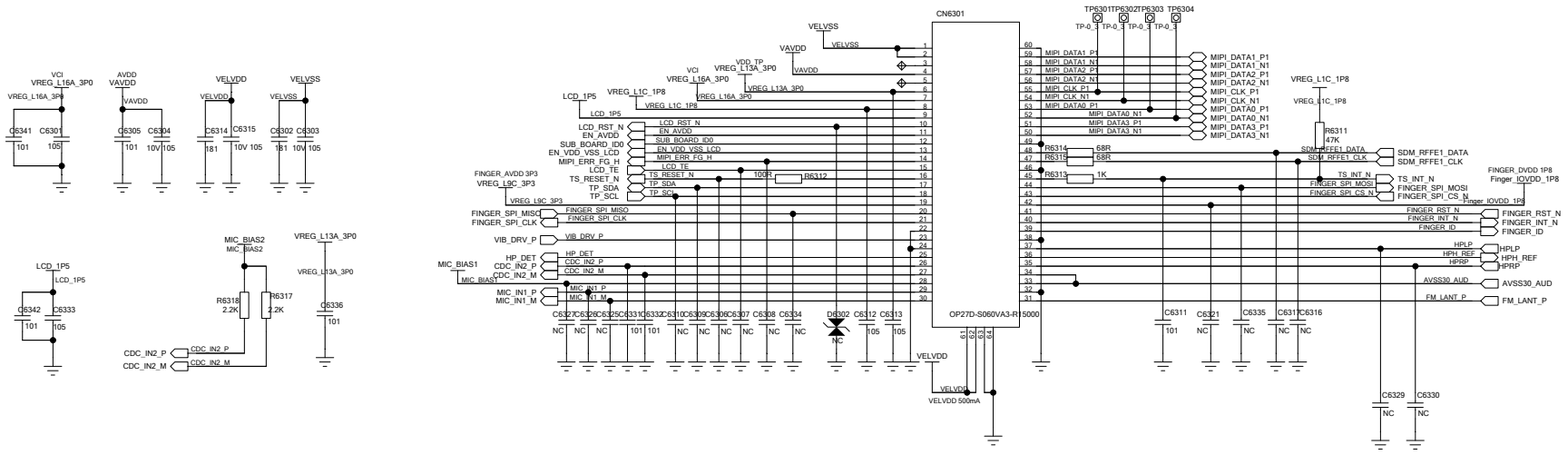
TFA9873 I2C Address (R:0x69; W:0x68)

	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet of 32	Ver:
Standard By			oppo	
Approved By				

DSI CMF

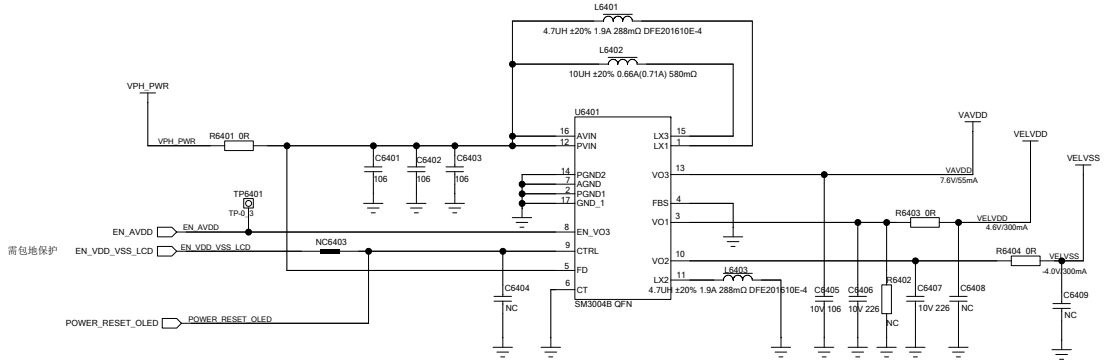


TO_L_FPC



	Sign	Date	Type:	
Drawn By			Draw No: A2SHEET	
Checked By			Sheet of 2	Ver:
Standard By			oppo	
Approved By				

OLED Driver



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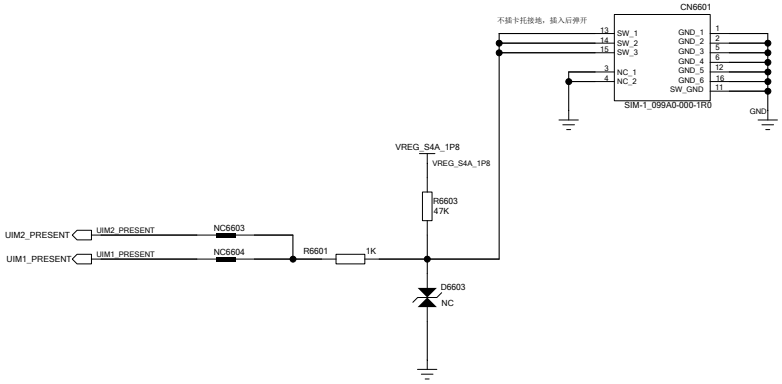
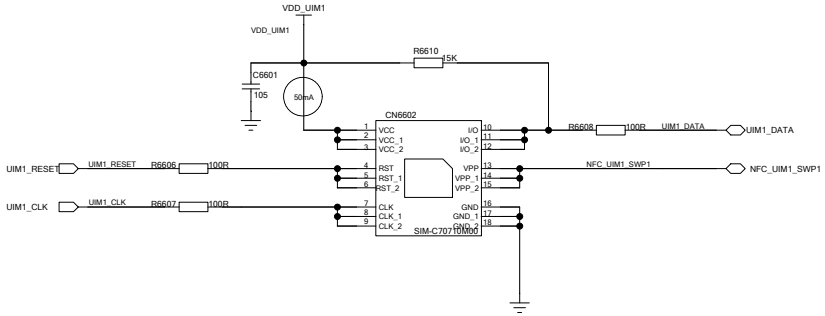
Standard By			oppo	
Approved By				

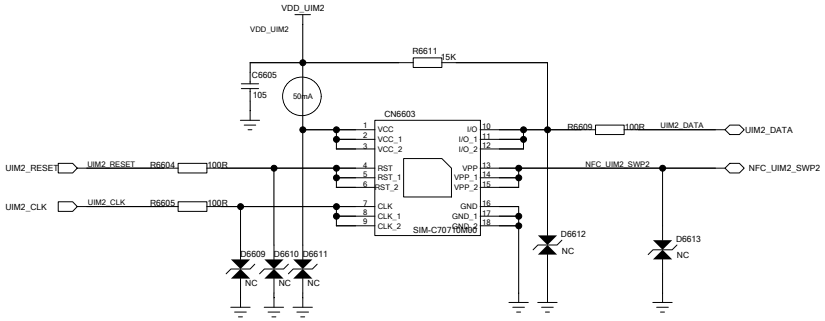
Plug Detect



SIM1 Card



SIM2 Card



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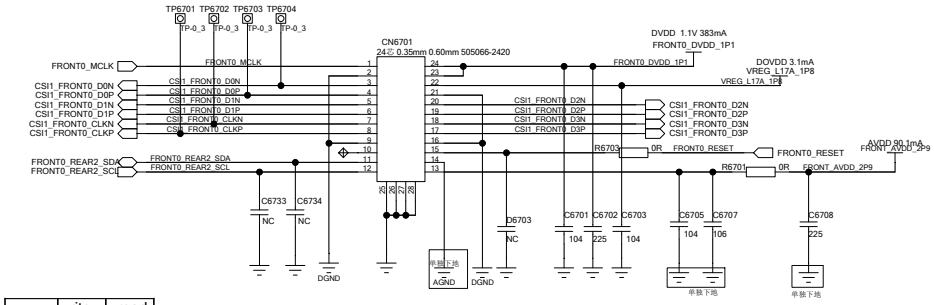
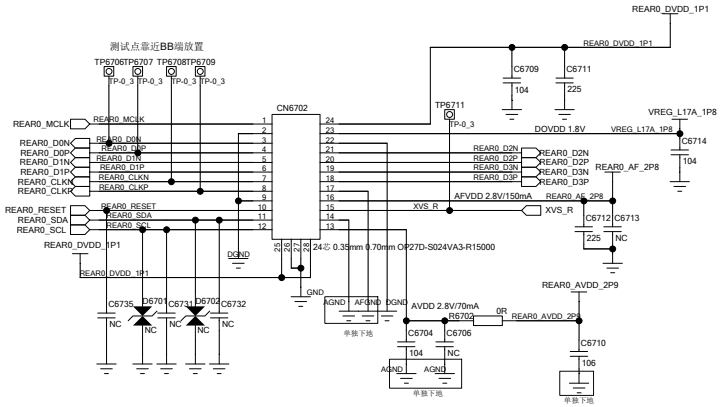
Checked By			Sheet 40_SIM_SD of 32	Ver:
Standard By			oppo	
Approved By				

Front0_Camera 32M



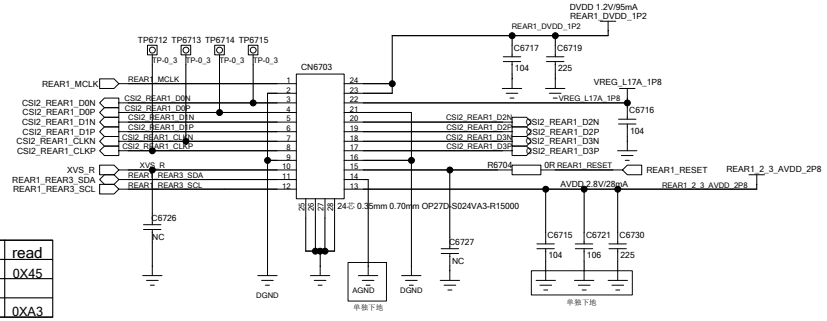
IMX616	write	read
sensor	0X20	0X21
EEPROM	0XA8	0XA9

Rear0_Main CAMERA 64M



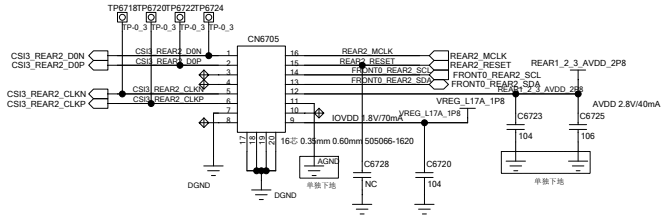
A64V04A	write	read
sensor	0X6C	0X6D
AF DRIVER	0X18	0X19
EEPROM	0XA0	0XA1

Rear1_Sub CAMERA 8M-FF



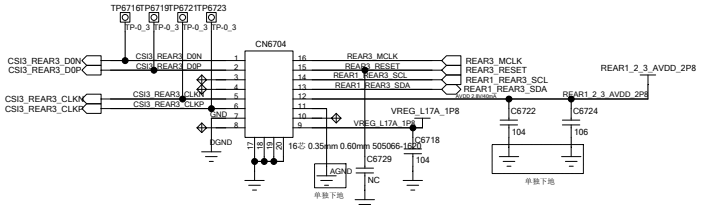
Hi646	write	read
sensor	0X44	0X45
driver		
EEPROM	0XA2	0XA3

Rear2_Camera(2M) MONO



GC02M1B	write	read
sensor	0X6E	0X6F
driver		
EEPROM	0XA4	0XA5

Rear3_Camera(2M) Micro



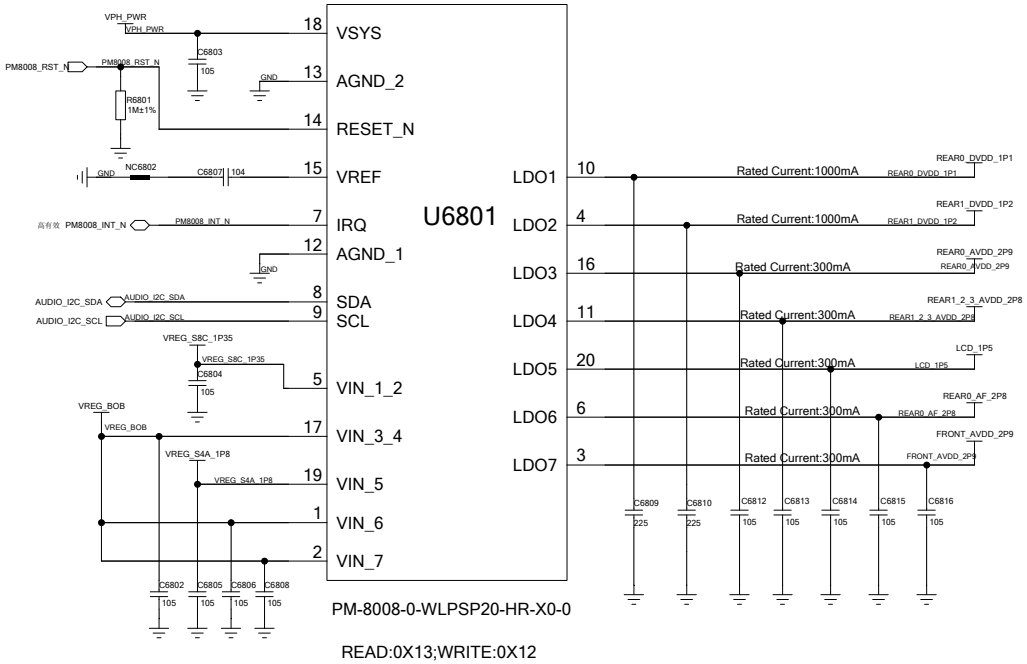
OV02B10	write	read
sensor	0X7A	0X7B
driver		
EEPROM	0XA4	0XA5

	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 55_MAIN_2nd_CAM_FLASH 2 Ver.
Standard By			oppo
Approved By			

PM8008

If VREG_BOB is used to supply any regulator input on PM8008, then VIN_7 must also have VREG_BOB as its input to the VMAX selector circuit for proper internal biasing.

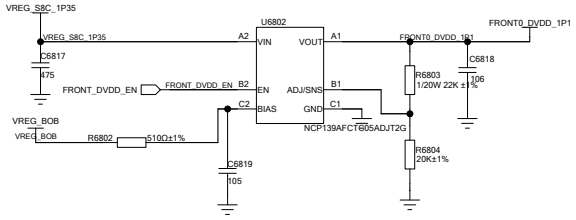
Ensure this equation is met for all regulators: Max (VSYS, VIN_7) >=max (VIN_X) over all conditions.



PM-8008-0-WLPSP20-HR-X0-0

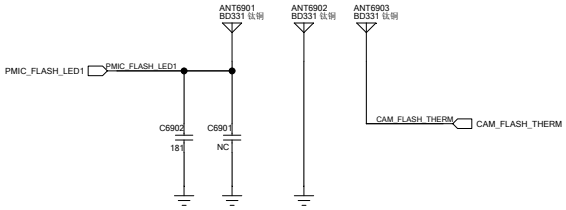
READ:0X13;WRITE:0X12

Front0_DVDD_1P05



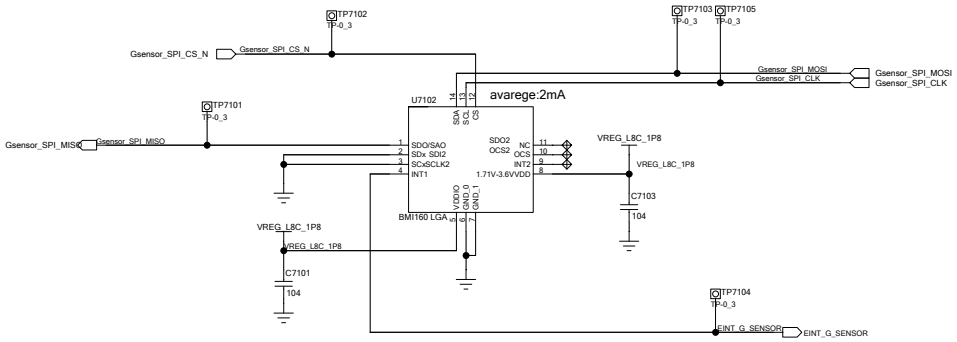
	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet of 52	Ver:
Standard By			oppo	
Approved By				

FLASH

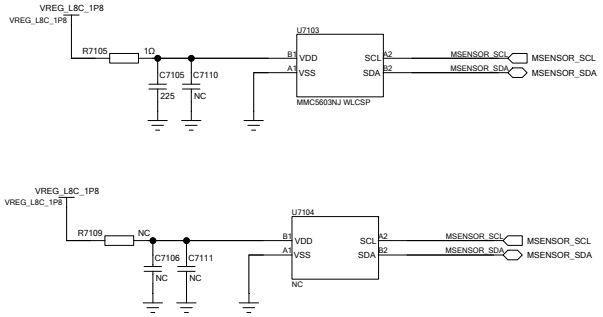


	Sign	Date	Type:
Drawn By			Draw No: Schematic1
Checked By			Sheet 55_MAIN_SUB_CAM_FLASH of 2 Ver.
Standard By			oppo
Approved By			

A+G SENSOR

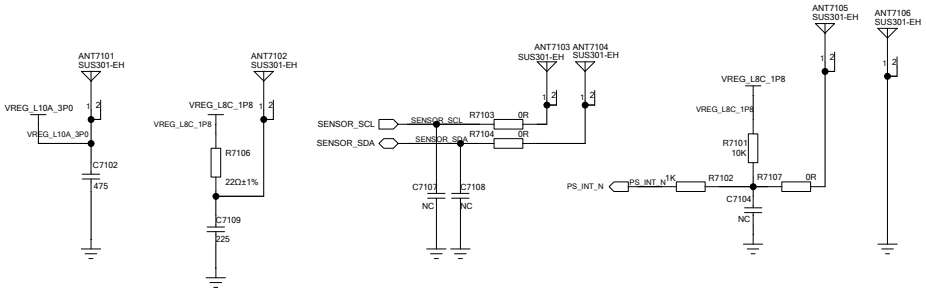


Magnetic Sensor



M-sensor	Read	Write
AK09918	0X19	0X18
MMC5603NJ	0X61	0X60

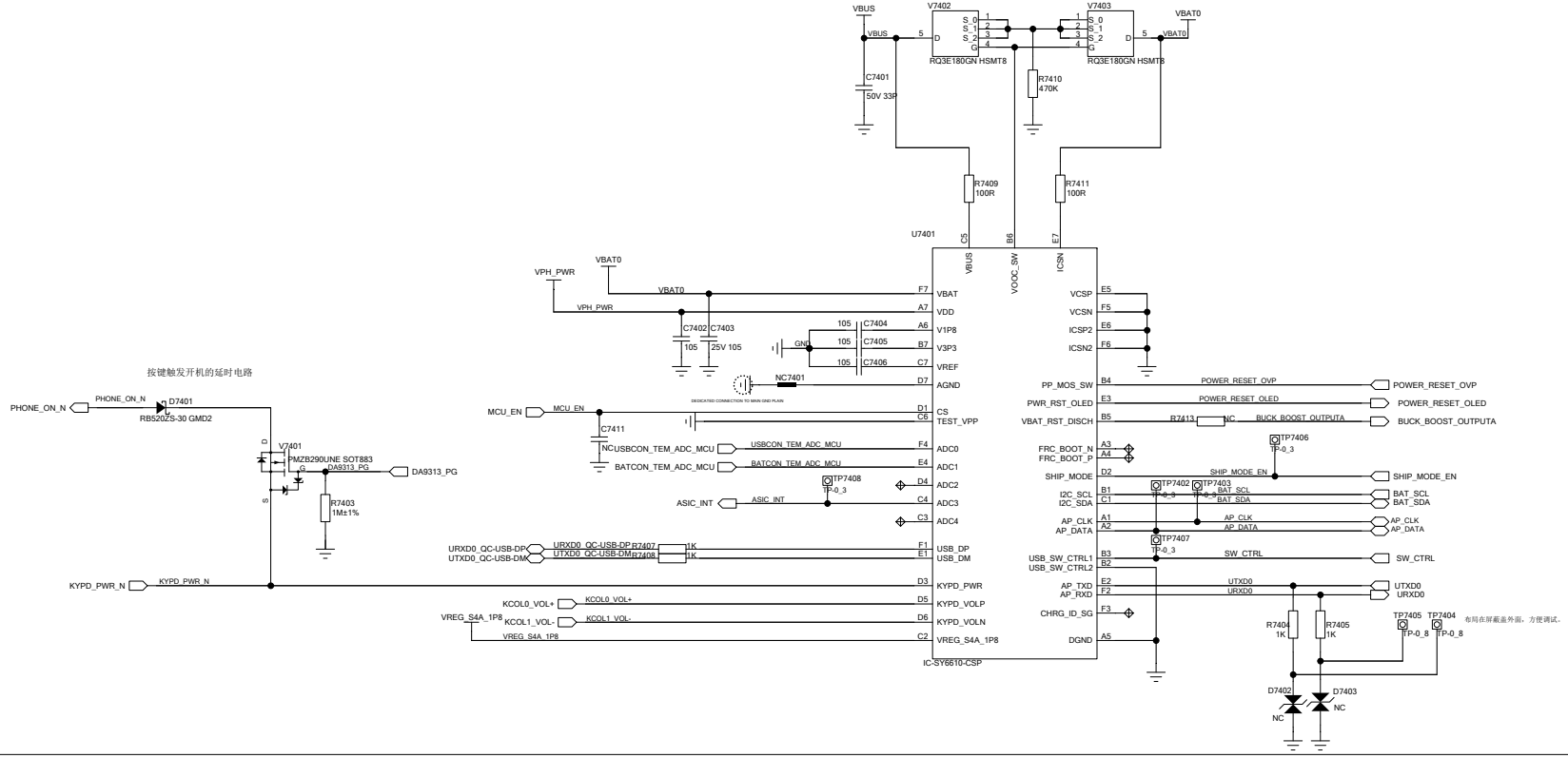
P.S+A.L.S sensor



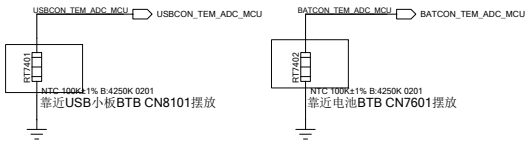
PS+ALS	Read	Write
TCS3701	0X19	0X18

	Sign	Date	Type:	
Drawn By			Draw No: A2SHEET	
Checked By			Sheet of 2	Ver:
Standard By			oppo	
Approved By				

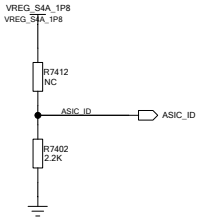
MCU



Thermistor

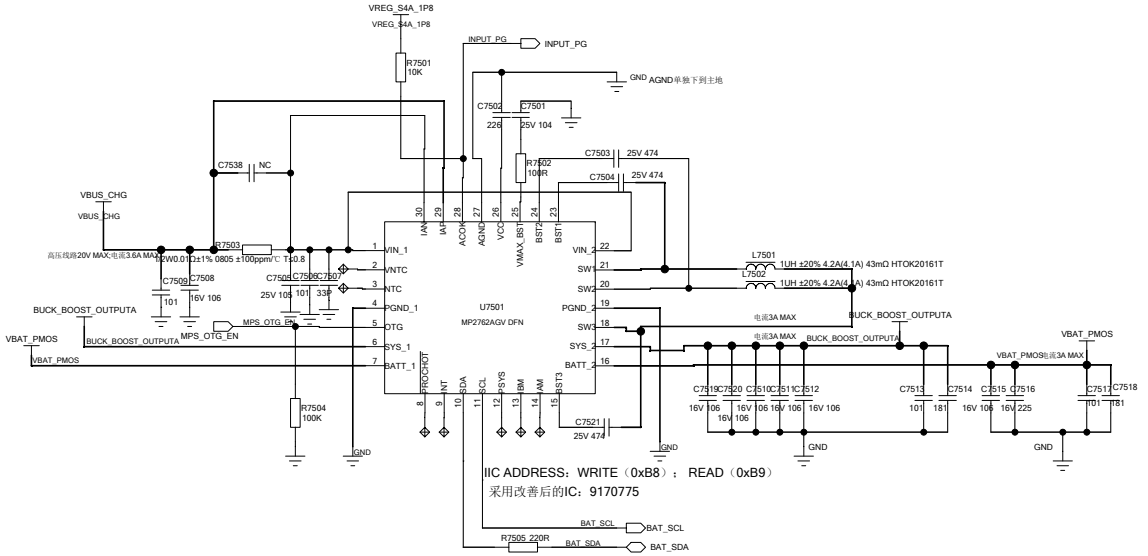


ASIC ID



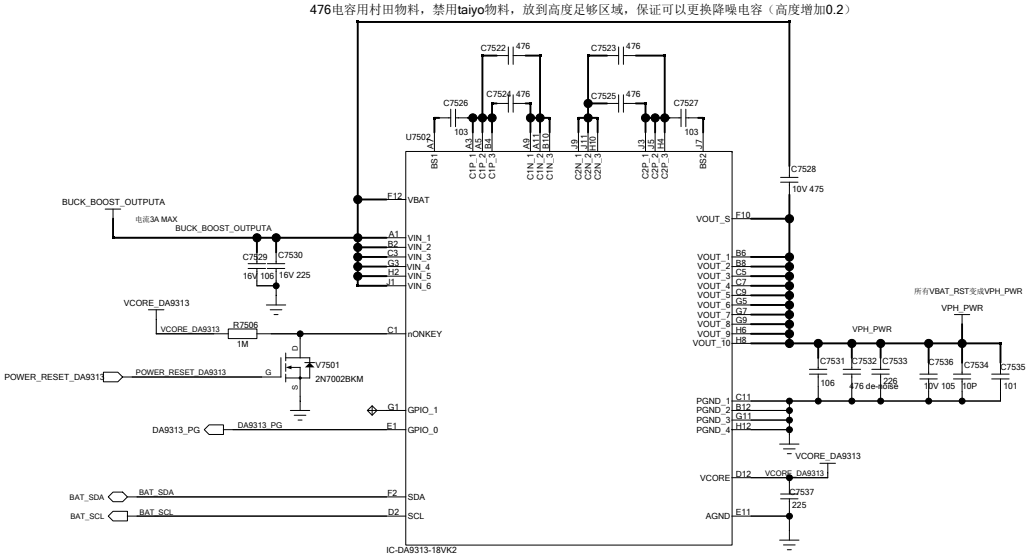
	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet 19_MCU_SWITCH_FAST_CHARGER of 19 Ver:
Standard By			oppo
Approved By			

BUCK-BOOST CHARGE



CHARGE PUMP

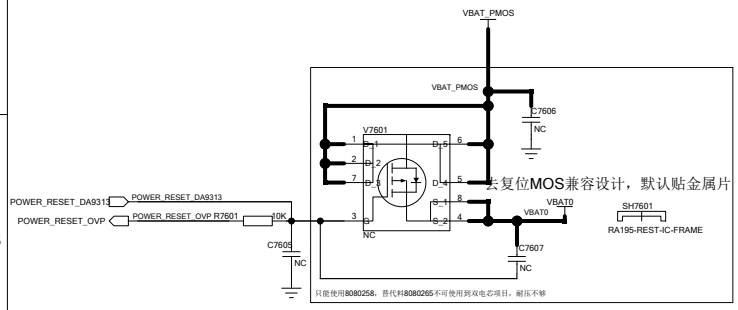
476电容用村田物料，禁用taiyo物料，放到高度足够区域，保证可以更换降噪电容（高度增加0.2）



DA9313 I2C Address (R:0xD1; W:0xD0)

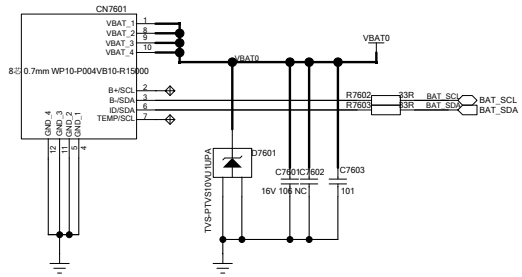
	Sign	Date	Type:	
Drawn By			Draw No:	Schematic1
Checked By			Sheet	53 of 64 Sheets 2
Standard By			Ver:	
Approved By			oppo	

HW RESET

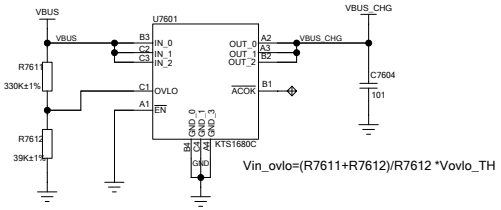


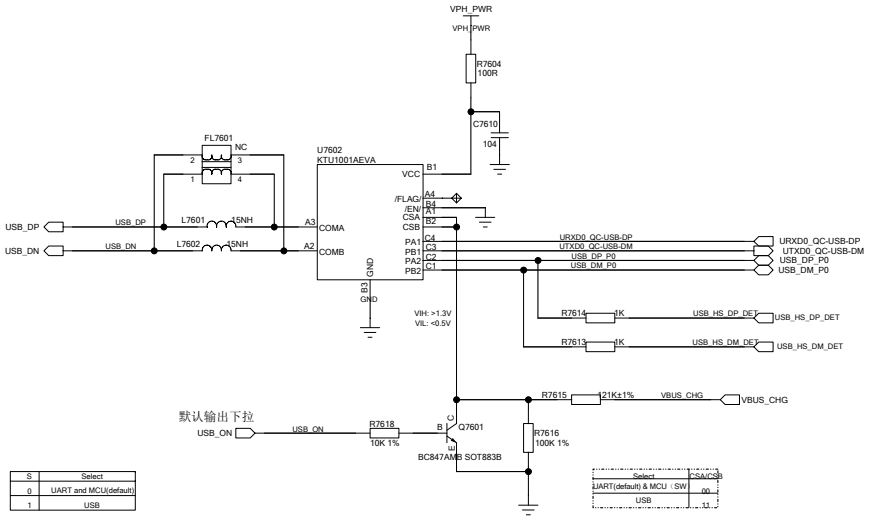
Battery Connector

8Pin Battery Con



USB OVP/SWITCH





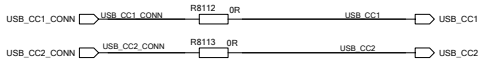
S	Select
0	UART and MCU(default)
1	USB

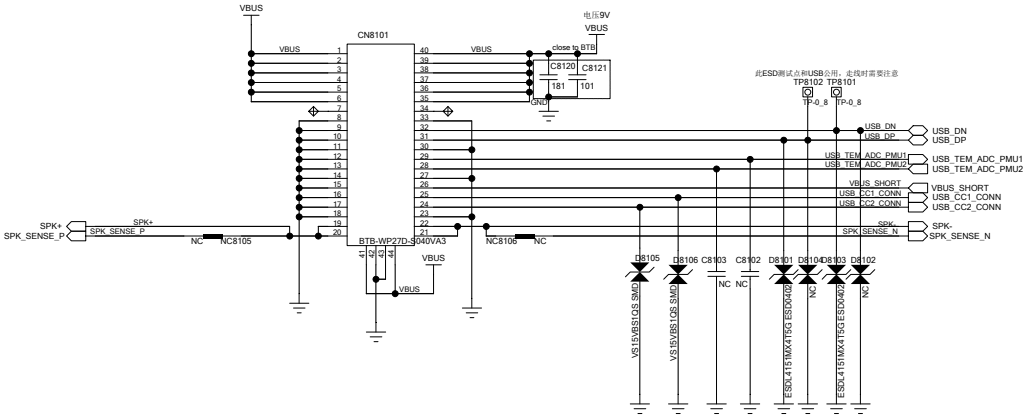
Select	CSA/CSB
UART(default) & MCU（SW	00
USB	11

	Sign	Date
Drawn By		
Checked By		
Standard By		
Approved By		

Type:
Draw No: Schematic
Sheet: 35_SW_RST_OVP_SWITCH
Ver:

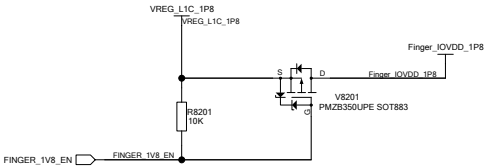
TO U_FPC





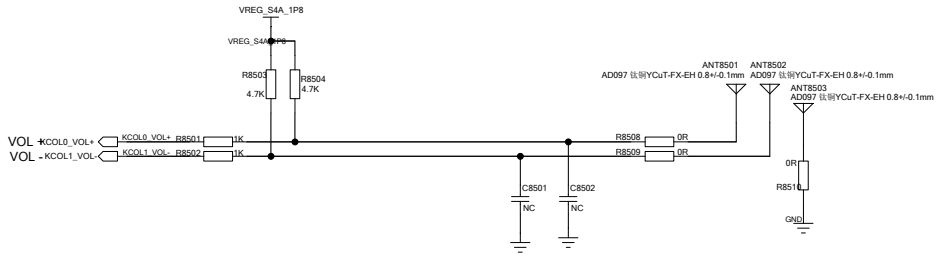
	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet 41 of	Ver:
Standard By			oppo	
Approved By				

Finger_IOVDD

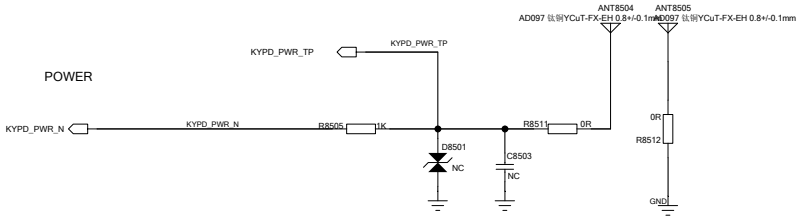


	Sign	Date	Type:	
Drawn By			Draw No: Schematic	
Checked By			Sheet of 41	Ver:
Standard By			oppo	
Approved By				

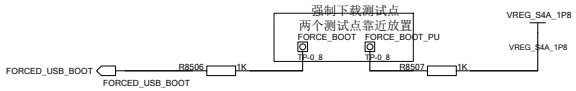
Key of Volume + -



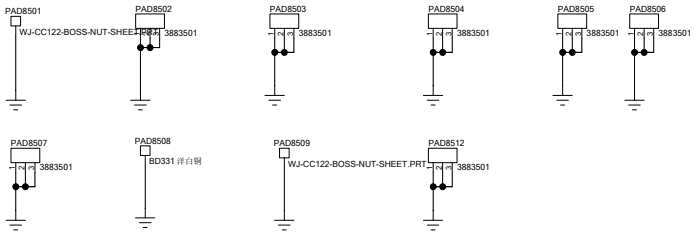
Power Key



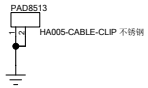
Force_USB_Boot



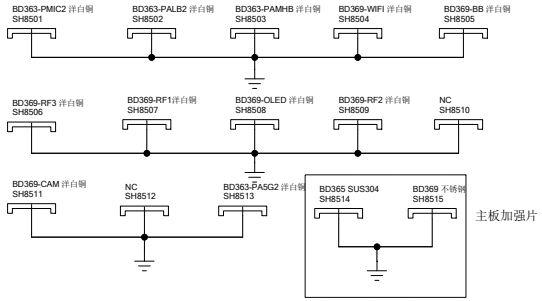
螺钉垫片



RF线夹

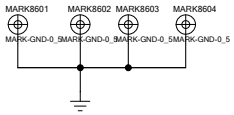


屏蔽支架



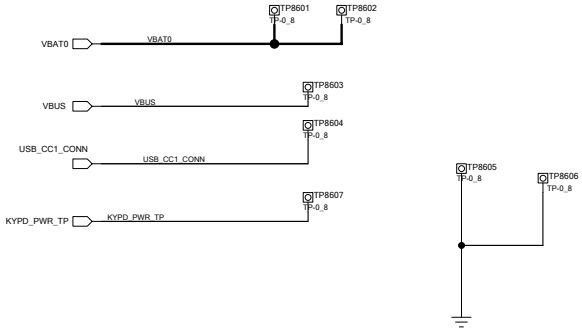
	Sign	Date	Type:	
Drawn By			Draw No: Schematic1	
Checked By			Sheet of 52	Ver:
Standard By			oppo	
Approved By				

MARK POINT

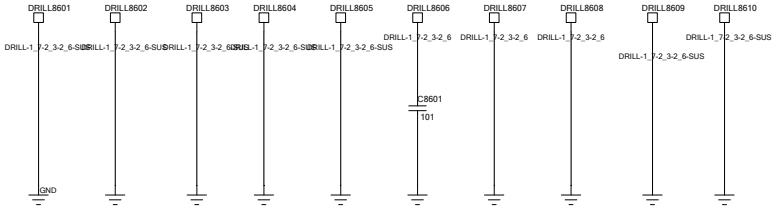


Test Point

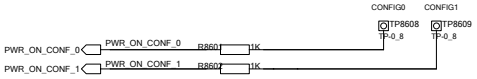
全功能测试点



主板螺钉孔



Test Config



综测校准测试点

BOOT MODE

CONF_0	CONF_1	Mode
0	0	Factory Mode
0	1	WLAN Final Test
1	0	RF mode
1	1	Ordinary Power On

	Sign	Date	Type:
Drawn By			Draw No: Schematic
Checked By			Sheet: 20_USB_SWITCH_KEY_TEST Of: 1 Ver:
Standard By			oppo
Approved By			